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Optimization of Two-Stage Operational Amplifier Using Firefly Algorithm Considering Environmental Constraints

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Abstract: Nature inspired algorithms are simple, efficient, and well-organized evolutionary computational techniques to optimize the design process of Analog electronic circuits. Due to the presence of several competitive design objectives, analog circuit sizing is inadequate without the analysis of trade-offs between the performance specifications. Therefore proposed work adopted firefly optimization, to optimize the design of the Operational Amplifier by optimising the various design specifications like Gain, Slew Rate, etc., involved in the design to achieve the comprehensive goal of minimum transistor required in the design. The designed two-stage operational amplifier is implemented in UMC 0.18 μm CMOS technology using CADENCE software. Experiments were carried out taking into consideration the design constraints, for different ranges of design variables and were also verified by comparing with simulated results from CADENCE. Based on these results, it can be said that firefly algorithms can match up to theoretical and simulated results, with the firefly algorithm being able to achieve better results in terms of better optimum values of design specification such as Gain, Slew Rate, etc.

Key words: Evolutionary algorithm, firefly algorithm, analog circuit, operational amplifier, optimisation techniques, temperature.

Introduction

Prompt developments happened in the technology field, resulting in the demand for optimised Analog /mixed VLSI circuits design, to comprise more characteristics on SoC (System-on-a-Chip). With the present trend complexity of analog circuit design is simultaneously steepened and necessitated a novel technique unlike the traditional technique, which carries much deficit concerning optimised output. The analog circuit has several degrees of freedom in terms of performance analysis with multi-dimensional solution space. The prime way to work in multi-dimensional solution space Analog circuit design is to invoke automation. The automated design of the Analog VLSI circuit has come to prominence from scientists (Nam et al., 2001).

The classical optimisation techniques are appropriate for analogue circuit sizing. For analog circuit optimisation, several classical optimisation techniques can be widely categorised as (Aarts et al., 2003) the Deterministic optimisation approach and the Stochastic Search approach (Martens et al. 2008). The Deterministic optimisation technique can easily find the global optima of any hard problem excellently,

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including the Branch and Bound technique (Doig et al., 1960), Simplex method (Nelder et al., 1965), Dynamic programming (Bellman et al., 2003), Goal Programming (Scniederjans et al. 2002), Numerical algorithm, etc. However, they are computationally complex so do not provide an excellent result for Non-deterministic Polynomial optimisation problems. In contrast, the Stochastic methods can provide better results without exploring abundant search space. However, they tend to converge towards a local optimum (Talbi et al., 2002). Therefore, the classical optimisation techniques are suitable for analog VLSI circuit sizing problems. To defeat the limitation of the classical optimization techniques, various Heuristics based and Metaheuristics-based optimisation has been suggested in the literature survey (Aarts et al., 2003). One of the most important motives for their popularity is that they have the adaptability characteristic as per the requirement of problems. Although they might be inefficient to achieve the exact optimum, they impart a solution having very close proximity to it (Petrowski et al., 2006). The heuristic-based mathematical optimisation techniques like Local Search (LS) (Glover et al., 1999), Genetic Algorithm (GA) (Bonabeau et al., 1999), Scatter Search (SS) (Kennedy et al., 1995), Simulated Annealing (SA) (Bonabeau et al., 1999), Tabu Search (TS) (Dorigo et al., 1999). However, the complexity of these methods increases with proportions of solution space and these are parameter sensitive. Therefore, to solve real-life problems and complex engineering problems, a bio-inspired heuristic-based optimization technique is defined. It has triggered the development of global solutions algorithm inspired by Swarm Intelligence (SI). Swarm Intelligence (SI) is the aggregate behaviour of natural or artificial, decentralised, and self-organized systems (Yang et al., 2013). Most of the popular SI techniques are Particle Swarm Optimisation) Ant Colony Optimisation, Artificial Bee Colony optimisation, Firefly Algorithm (FA) (Vural et al., 2012). PSO is the most popular, superior among its predecessors, and basic form of SI optimisation algorithm, which is used from a decade back and has performed efficiently in various fields (Kumar et al., 2016). The evolution of different computer-aided design (CAD) tools beginning from equation-based to simulation-based has been reported in Gielenanad Rutenbar.

In this work, the authors have tried to optimise the parameters of a two-stage operational amplifier. A Firefly Algorithm (FA) is utilised to optimise the parameters of a two-stage operational amplifier like Gain, CMRR, ICMR, and Slew rate. In this work, the Gain is maximised incorporating all necessary design constraints. Works of literature reveal that Firefly Algorithm has not been applied to date to optimize the above-said parameters of a two-stage operational amplifier. Hence this work is the first attempt to optimise the parameters of a two-stage operational amplifier using the Firefly Algorithm. The work is simulated in MATLAB version 2017b, with an i5 processor and 8 GB RAM and CADENCE Spectre, UMC, 180 nm technology.

This work aims to analyse and validate the performance of Firefly on the automation of analog circuit sizing problems considering the minimisation of MOS Transistor Area for Op-amp circuits. This work is arranged in the following sections: Procedure for Two-Stage Opamp Design – the systematic design procedure of the two-stage Operational amplifier is discussed and the objective function is formulated, Firefly Based Analog Circuit Design applications of a firefly in the optimum design of an analog circuit are discussed; Simulation Results for CMOS Two Stage Operational Amplifier – the simulation results are mentioned, followed by recognition of the system performance with the simulator tool CADENCE VIRTUOSO; and finally the Conclusion.

Procedure for Two-Stage Opamp Design

The area of Analog Circuit Design is very complex and required special designing skills for complicated circuitry. The CAD Tools for automated Analog circuit design are underdeveloped as compared to their digital counterpart because the analog design technologies are more probing and analytical.

In the present work, we study designing a CMOS two-stage operational amplifier for optimal performance as shown in Figure 1.

The design specifications which describe the circuit are:

- Common Mode Rejection Ratio (CMRR).
- Slew Rate (SR).
- Power dissipation (P_{diss}).
- Small-signal characteristics (A_v, f_1, f_{-3dB}).
- Input Common-Mode Range (ICMR).
- Unity Gain Bandwidth (UGB).

In this work, the design objective which is also defined as Cost Function (CF) is the minimisation of the overall MOS transistor area given as:

$$Minimise,\ CF = \sum_{k=1}^{T} W_k\, L_k \tag{1}$$

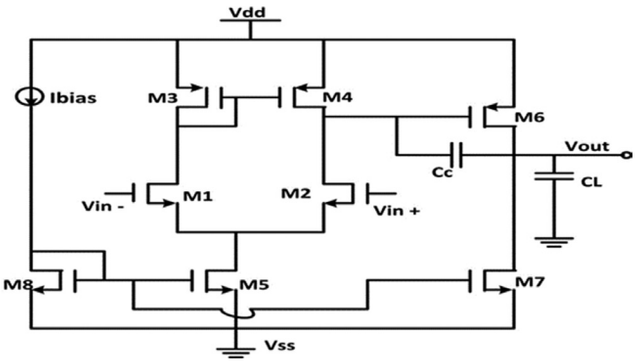

Figure 1: Two-stage CMOS operational amplifier.

where T is the total number of transistors, W_k and L_k represent width and length of the transistor which have to be determined using the design specifications such as small-signal differential voltage gain (A_v), unity-gain bandwidth (f_t), cutoff frequency (f_{-3dB}), minimum and maximum input common-mode range voltages (V_{ICMIN} and V_{ICMAX}), slew rate (SR), power dissipation (P_{diss}), keeping in view certain constraints, which are determined by the designer and the design rules which relate to them. As mentioned in the circuit diagram the value of k is from 1 to 8. T is the total number of the transistor. The design procedure followed to satisfy the constraints W and L of every transistor for specifications like Gain, ICMR, SR, etc and two-stage operational amplifier's objective are summarised below:

$$\left(\frac{W_3}{L_3}\right)=\left(\frac{W_4}{L_4}\right) \times\left\{\frac{I_{D5}}{K_p\left[V_{DD}-V_{IC(\max)}-\left|V_{tp\ (\max)}\right|+V_{tn\ (IC\min)}\right]^2}\right\} \quad (2)$$

$$\frac{W_5}{L_5}=\frac{W_8}{L_8}=\frac{g_{m1}}{K_n\left[V_{DS5(sat)}\right]^2} \quad (3)$$

$$\frac{W_1}{L_1}=\frac{W_2}{L_2}=\frac{g_{m1}^2}{K_n I_{D5}} \quad (4)$$

$$\frac{W_6}{L_6}=\frac{W_4}{L_4}\left(\frac{g_{m6}}{g_{m4}}\right) \quad (5)$$

$$\frac{W_7}{L_7}=\frac{W_5}{L_5}\left(\frac{I_{D6}}{I_{D5}}\right) \quad (6)$$

where, $I_{D5} = SR \times C_c$,

$$V_{DS5(sat)}=V_{IC(\min)}-V_{SS}-V_{tn\ (\max)}-\sqrt{\frac{I_{D5}L_1}{K_n W_1}}$$

$$g_{m1} = 2\pi UGBC_c \text{ and } g_{m6} \geq 10\ g_{m1}$$

The above equations along with the constraints are utilised by firefly algorithms, to achieve the optimum size of the MOSFETs so that the Cost Function is minimised.

Firefly Based Analog Circuit Design

The firefly algorithm provides a good balance of exploitation and exploration (Kumar et al., 2018).

Firefly Algorithm (FA) was developed by Xin-She Yang in late 2007 and 2008 at Cambridge University based on the flashing patterns, the phenomenon of bioluminescent communication and behaviours of tropical fireflies at night. Fireflies are winged beetles that produce light and blink at night. Firefly Algorithm is a bio-inspired metaheuristic algorithm for optimisation techniques. Fireflies produce light that has a visible frequency which is bio-chemically produced called bio-luminescence. The main motivation behind the advanced metaheuristic algorithms is Natural selection and Survival of the fittest. Fireflies use their flashing patterns to communicate during the night for food searching, to attract their mate, and also to warn predators. For the accurate representation of the behaviours of fireflies, Xin She Yang considered the following mathematical assumptions for the evolution of the firefly algorithm (Yang et al., 2013).

1. Fireflies are unisexual, so every firefly will attract one another regardless of their sex.
2. The attractiveness and brightness of fireflies are directly proportional. Also, they both are inversely proportional to distance. Hence, for two flashing fireflies, the least brighter one will be captivated by the brighter firefly. If no brighter firefly is found than a particular firefly, both (it) will move randomly.
3. The brightness of a firefly is made associated with the value of the objective function; so, for a maximization problem, the brightness can simply be proportional to the value of the objective function.

To analyse the performance of firefly algorithms in the optimal design of the analog circuit and to compare their operation, two fundamental analog circuit structures have been considered. The assignment of both algorithms is to achieve the optimal dimensions

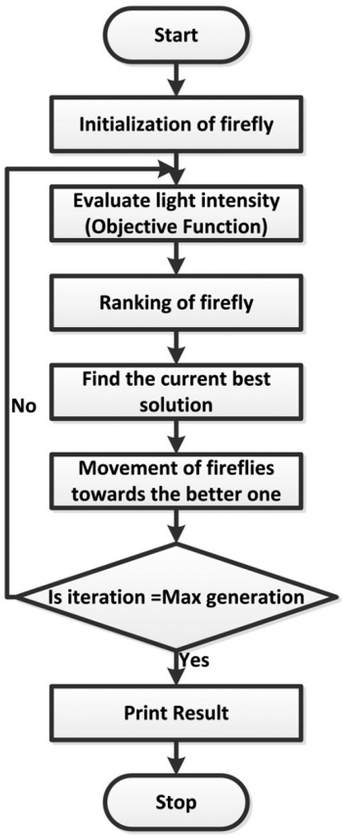

Figure 2: Flowchart of firefly algorithm.

of MOS transistors, such as minimisation of CF defined in Equation (1), as satisfying the design parameter constraints and design specifications.

First of all, the optimisation process depends on two facts, one is the power supply value and the technology considered by the researcher and the other is the design criteria. The design specifications, the design parameters range, values of power supply, and technology information are considered as inputs to both the optimisation techniques. The assignment of the algorithms is to achieve the optimal value of the design parameters (C_L, C_c, $\frac{W_i}{L_i}$), for CMOS differential amplifier with current mirror load i=1, 2…6 and for CMOS two-stage Op-amplifier=1,2,…..8 and design specifications [SR, $V_{IC(MAX)}$, $V_{IC(MIN)}$, $f(-3dB)$, f_t) within the specified ranges. The circuit simulations are carried out with CADENCE VIRTUOSO with model parameters of United Microelectronics Corporation (UMC) 180Å technology for validation purposes. The technology parameters values used in the design are shown in Table 1.

Table 1: Topology, inputs, and lengths considered of UMC 180

Specifications	V_{dd} (V)	V_{ss} (V)	V_{tp} (V)	V_{tn} (V)	K_n ($\mu A/V^2$)	K_p ($\mu A/V^2$)
Values used	1.8	-1.8	-0.42	0.42	355	75

Firefly Algorithms are programmed using MATLAB 2017a that runs on a CPU Intel Core i7 with 8GB RAM. The design variables for the CMOS two-stage Op-amp structure are defined in Equation (7). For the optimisation problem, the design vector is as given:

$$X_{opamp} = \left[SR, C_L, A_v, f_t, \mathrm{V}_{IC\,min}, V_{IC\,\max}, P_{diss} \right] \quad (7)$$

where slew rate (SR) is expressed in (V/μs), output capacitance (C_L) in pF, Gain (A_v) in dB, Unity Gain Bandwidth (f_t) in MHz, the minimum and maximum values of the ICMR are (V_{ICmin}) in (V) and (V_{ICmax}) in (V) and Power dissipation (P_{diss}) in μW, respectively.

Simulation Results for CMOS Two Stage Operational Amplifier

Regarding Op-amp design, (i) two-stage Op-Amp is considered and (ii) firefly algorithm has been used for obtaining the optimum value of circuit design parameters that satisfy the design specifications and are as below:

SR ≥ $10\frac{V}{\mu s}$, $A_v > 10^3 \frac{V}{V}$, $f_t \geq$ 3MHz, -1.5V ≤ ICMR ≤ 2V, $P_{diss} \leq$ 2500 μW and the constraint for the design are: Load Capacitance (C_L) is kept as $C_L \geq$ 7pF and aspect ratio is kept as $100 \geq (W/L)_k \geq 2$ for all k except k = 5, 8 where it is $100 \geq (W/L)_k \geq 1$. To minimise Channel Length Modulation, we have chosen $L_1 = L_2 = L_3 = L_4 = L_5 = L_6 = L_7 = L_8 = 2$ μm. The two Stage OP-AMP have been simulated in the CADENCE VIRTUOSO simulator.

In this section design solution obtained by Firefly Algorithm is utilised to obtain the parameters of a two-stage operational amplifier like Gain, Slew rate, ICMR, and CMRR. The simulated results are shown in Figures 2 to 5. Figure 3 shows that the value of Gain is 77.66 dB. The circuit design parameter values calculated through the algorithm, after meeting both design specifications and the area constraints are given in Table 2. The results of the firefly algorithm by design specifications are given in Table 3. The CADENCE VIRTUOSO simulation plots in Figures 2 to 6 declare (reveal) that the design based on the algorithm satisfies design criteria and all specifications.

Table 2: Design parameters obtained with firefly for the Op-Amp

Design Parameters	I_{bias} *(μA)*	C_c *(pF)*	W_1/L_1	W_2/L_2	W_3/L_3	W_4/L_4	W_5/L_5	W_6/L_6	W_6/L_6	W_8/L_8
Firefly Algorithm	25	2	4/2	4/2	4/2	4/2	4/2	14.5/2	7.25/2	4/2

Table 3: Optimised parameters obtained in CADENCE

Specifications	*Slew rate (V/μs)*	*Avg power*	*Gain (dB)*	F_t *(MHz)*	V_{ICmin} *(V)*	V_{ICMAX} *(V)*	*Total area* (μm_2)
Simulated Results	31.6	109.3uw	77.66	3.1	-0.293.5	1	98

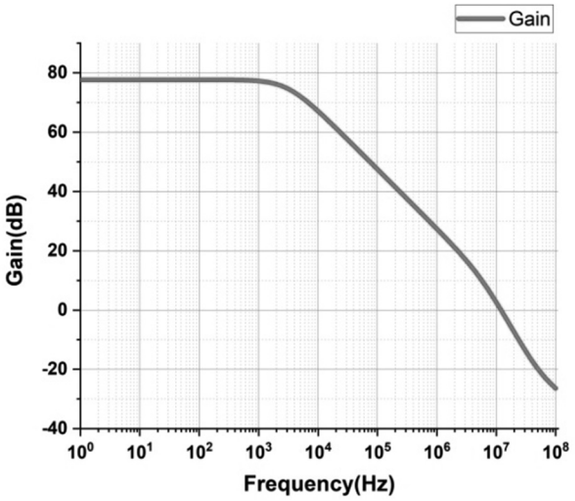

Figure 3: Gain plot of Opamp.

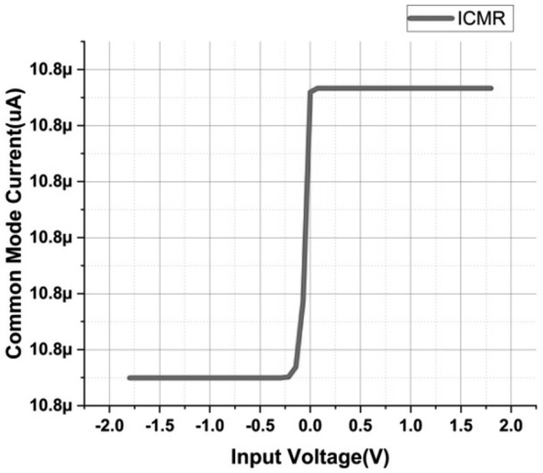

Figure 5: ICMR plot of operational amplifier.

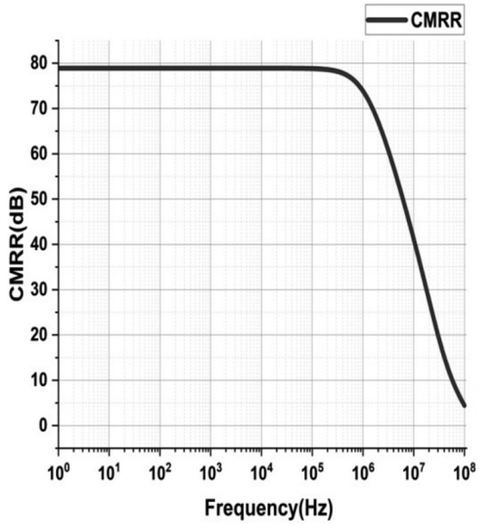

Figure 4: CMRR Plot of Opamp.

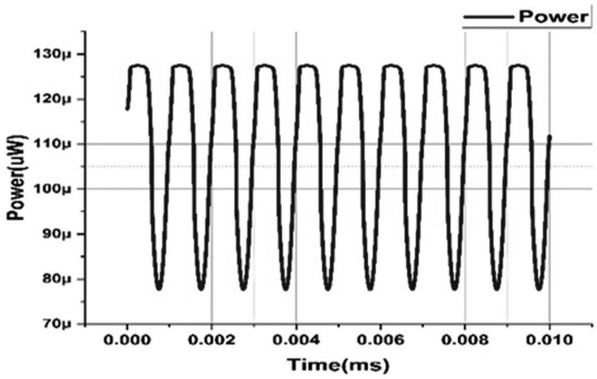

Figure 6: Dynamic power plot of operational amplifier.

Conclusion

In this work, a highly effective algorithm from the swarm family called Firefly is used to optimize the CMOS two Stage Op_{amp} parameter. The result achieved through the firefly algorithm found that the area obtained by the algorithms is better than the earlier works for the CMOS two Stage Opamp. Firefly algorithm simulated results had improved values for optimum results for design variables like Slew rate, Gain, and Power dissipation. For validation of the results, the OP-AMP is redesigned in the standard circuit simulator CADENCE VIRTUOSO implementing the values of design variables as DC bias current and Width of MOS transistor, obtained by the firefly algorithm. When simulated using CADENCE software, the value of Gain, Slew rate are found to be 77.66 dB and

31.6 V/µs, respectively. The simulation results from CADENCE VIRTUOSO not only prove that firefly-based Analog Circuit Design converges design specifications and criteria, but it also verifies that the firefly has superior performance for Op-Amp than earlier reported results in terms of minimum Power dissipation, better Gain, CMRR, etc.

References

Aarts, E. and K. Lenstra (2003). Local search in combinatorial optimization, Princeton University Press.

Bonabeau, E., Dorigo, M. and G. Theraulaz (1999). Swarm intelligence: From natural to artificial systems. New York: Oxford University Press.

Bellman, R.E. (2003). Dynamic programming, Courier Corporation.

Doig, A.G. and A.H. Land (1960). An automatic method for solving a discrete programming problem. *Econometrica*, **28:** 497-520.

Dorigo, M., Carog, D. and L. Gambardella (1999). Ant algorithms for discrete optimization. *Artificial Life*, **5:** 137-72.

Glover, F. (1990). Tabu search-part II. *ORSA Journal on Computing*, **2(1):** 4-32.

Kennedy, J. and R.C. Eberhart (1995). Particle swarm optimization. *Swarm Intelligence*, **1:** 35-57.

Kumar, R., Rajan, A., Talukdar, F.A., Dey, N., Santhi, V. and V.E. Balas (2016). Optimization of 5.5-GHz CMOS LNA parameters using firefly algorithm. *Neural Comput Appl*, **28:** 1-15.

Kumar, R., Talukdar, F.A. and A. Rajan (2018). Parameter opt2(1)imization of 5.5 GHz low noise amplifier using multi-objective firefly algorithm. *Microsyst. Technol*., **26:** 3289-3297.

Martens, E. and G. Gielen (2008). Classification of analog synthesis tools based on their architecture selection mechanisms. *Integr VLSI J*., **41(2):** 238-252.

Nam, D., Seo, Y., Park, L., Park, C. and B. Kim (2001). Parameter optimization of an on-chip voltage reference circuit using evolutionary programming. *IEEE Trans Evol Comput*, **5(4):** 414-421.

Nelder, J.A. and R. Mead (1965). A simplex method for function optimization. *Computer Journal*, **7(4):** 303-318.

Petrowski, J.D.A. and P.S.E. Taillard (2006). Metaheuristics for Hard Optimization. Springer.

Scniederjans, M.J. (1995). Goal programming methodology and applications.

Talbi, E.G. (2002). A taxonomy of hybrid metaheuristics. *Journal of Heuristics*, **8:** 541-564.

Vural, R.A. and T. Yildirim (2012). Analog circuit sizing via swarm intelligence. *AEU International Journal of Electronics and Comm*, **66:** 732-740.

Yang, X.S. (2013). Firefly algorithm: Recent advances and applications. *Int. J. Swarm Intelligence*, **1:** 36-50.