ACCSCIENCE PUBLISHING

Design+

ARTICLE

High-speed comparator-based switched-capacitor circuit with non-linear current source for photodiode detector applications

Amir Ali Mohammad Khani[1], Ilghar Rezaei[2], Ava Salmanpour[3], and Toktam Aghaee[4]*

[1]Department of Electrical Engineering, Sav. C., Islamic Azad University, Saveh, Iran

[2]Department of Electrical Engineering, CT. C., Islamic Azad University, Tehran, Iran

[3]Department of Electrical Engineering, Shahid Chamran University, Ahvaz, Iran

[4]Department of Electrical Engineering, Semnan University, Semnan, Iran

Abstract

In scaled complementary metal–oxide–semiconductor (CMOS) processes, op-amp-based switched-capacitor photodiode readouts face intrinsic-gain and bandwidth limitations, motivating comparator-based switched-capacitor (CBSC) architectures that use fast comparators and current-driven charge transfer for high-speed, low-power operation. This paper introduces a novel CBSC circuit architecture designed to enhance photodiode readout performance. Unlike conventional designs that rely on high-gain operational amplifiers, the proposed approach leverages a non-linear current source to trigger a comparator, enabling virtual-ground formation and high-speed charge transfer. The circuit was implemented and evaluated via HSPICE simulations in a 0.18 μm CMOS technology and demonstrated reliable operation at frequencies up to 100 MHz. Key innovations include a non-linear current-source scheme to accelerate the photodiode voltage response and a reset mechanism that further reduces operational delay. Detailed simulation results confirm robust, power-efficient operation with tolerance to temperature and process variations. These findings suggest that the proposed CBSC circuit is a promising, energy-efficient alternative for next-generation analog and mixed-signal sensor applications where high-speed pixel response is critical.

Keywords: Comparator-based switched-capacitor circuits; Photodiode detector; Non-linear current source; CMOS analog circuit design; High-speed sensor interface

***Corresponding author:**
Toktam Aghaee
(toktam.aghaee@semnan.ac.ir)

Citation: Khani AAM, Rezaei I, Salmanpour A, Aghaee T. High-speed comparator-based switched-capacitor circuit with non-linear current source for photodiode detector applications. *Design+*. 2026;3(2):025400043.
doi: 10.36922/DP025400043

Received: October 5, 2025

Revised: February 3, 2026

Accepted: February 12, 2026

Published online: March 31, 2026

1. Introduction

Comparator-based switched-capacitor (CBSC) circuits represent a rapidly advancing class of analog and mixed-signal circuit design, offering innovative solutions to the limitations introduced by aggressive technology scaling in contemporary scaled complementary metal–oxide–semiconductor (CMOS) processes.[1] Classical switched-capacitor circuits relied heavily on high-gain operational amplifiers (op-amps) to enforce a virtual-ground condition necessary for accurate charge transfer. This dependence has become increasingly problematic as device dimensions decrease and the achievable intrinsic gain of transistors declines.[2] Constraints on op-amp performance not only affect

transfer fidelity and speed but also complicate stability and compensation, posing challenges for robust circuit implementation in scaled CMOS technologies.[3]

The emergence of CBSC circuits provides a transformative alternative by substituting op-amps with comparators, which are inherently faster and more power-efficient. In CBSC operation, comparators detect the virtual-ground condition and initiate current-based charge transfer, thereby reducing reliance on high-gain amplification and feedback-based stabilization used in traditional architectures.[4] This approach unlocks several advantages: substantial reductions in power consumption, diminished complexity in compensation design, and robust operation across process, voltage, and temperature (PVT) variations. Accordingly, CBSC circuits are increasingly considered for widespread adoption in low-power, high-speed sensor interfaces, portable electronics, and mixed-signal systems, including analog-to-digital converters and delta-sigma modulators.[5,6]

In photodetector circuits, especially for high-frame-rate imaging and sensing, the limitations of conventional amplifier-based schemes are pronounced. Typical readout circuits for photodiode arrays utilize amplifiers to process charge accumulation and reset cycles, which can constrain pixel response time due to finite amplifier bandwidth and slew rate.[7] Reset mechanisms, integral to image-sensor operation, further restrict speed because charging and discharging of photodiode nodes hinge on the response of the entire analog chain. Recent research emphasizes that non-linear amplification and reset strategies that leverage comparator-triggered current sources can critically enhance pixel speed while limiting overshoot and power consumption.[8,9]

This paper presents a CBSC circuit with a non-linear current source engineered to accelerate the photodiode response and reduce comparator-triggering delay. Rather than a direct voltage-mode comparison to a reference level, the proposed configuration charges an intermediate node with a current proportional to the photodiode voltage, enabling a faster approach to the comparator threshold. A carefully designed reset phase presets the circuit closer to this threshold, thus further reducing operational delay. Importantly, multiple performance trade-offs are analyzed, including the balance among speed, comparator offset errors, and overall accuracy, reflecting the subtle interplay between non-linear response enhancement and system-level fidelity.[10]

While prior works have explored CBSC integrators[6,7] and non-linear charging schemes[7], this paper presents, to the best of our knowledge, the first application of a non-linear current source within a CBSC topology for photodiode detector readout, with an explicit focus on high-speed pixel response. Key innovations include a tailored reset scheme (V_{cal}) and a transistor-level non-linear source that accelerates comparator triggering beyond prior CBSC implementations.[11]

Today, mixed-signal circuits implementing switched-capacitor techniques must balance speed, noise performance, and power efficiency. These demands become especially acute at high operating frequencies due to aliasing, switching noise, and thermal noise effects.[12] The CBSC methodology, particularly its non-linear variants, directly addresses these obstacles by eliminating bandwidth bottlenecks and optimizing charge transfer with minimal complexity. The presented work thus contributes a scalable, energy-efficient readout platform for advanced photodiode arrays, relevant for next-generation imaging, biomedical, and sensor applications where frame rate and pixel accuracy are critical.[13]

The remainder of the paper is organized as follows: Section 2 describes the conventional photodiode readout scheme; Section 3 presents the proposed non-linear CBSC circuit; Section 4 discusses simulation results; and Section 5 concludes the paper and outlines directions for future research.

2. Conventional photodiode readout scheme

Figure 1 shows a conventional CBSC photodiode readout circuit In this scheme, the photodiode voltage (V_{pd}) is compared directly with a reference voltage (V_{ref}) using an op-amp-based comparator. During the reset phase, the reset switch (S_R) is closed, pulling V_{pd} to ground (rail voltage). During the integration phase, S_R opens, and the photodiode discharges linearly toward V_{ref}. The comparator triggers when V_{pd} crosses V_{ref}, producing a digital output pulse.

The primary limitations of this approach are:

(i) Linear voltage ramp: The ramp slope is constant, leading to a longer time to reach V_{ref}.
(ii) Full-swing reset to a supply rail: Resetting V_{pd} to ground increases the voltage swing required to reach V_{ref}.
(iii) Op-amp dependency: The op-amp's finite bandwidth and slew rate limit overall speed.

These factors constrain the maximum operational frequency (reported to be on the order of 10 MHz in 0.18 μm CMOS implementations). In this conventional scheme, the time required for V_{pd} to reach V_{ref} depends on the ramp set by the photodiode current and the effective capacitance at the node. The following section introduces

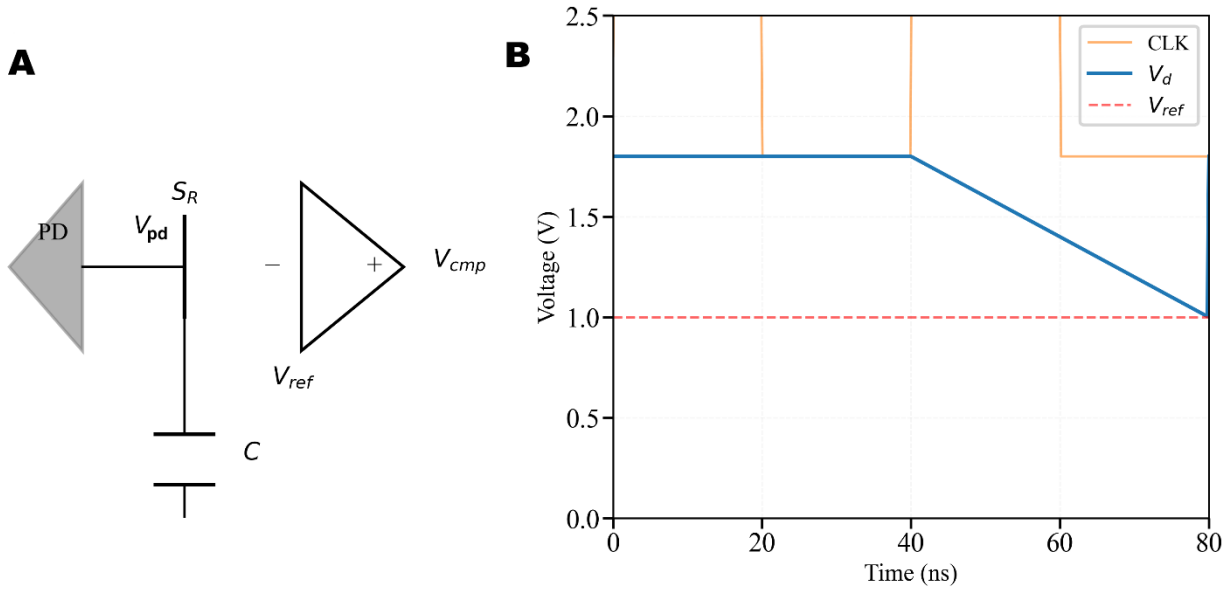

Figure 1. Conventional comparator-based switched-capacitor photodiode readout circuit. (A) Schematic showing photodiode (PD), reset switch (S_R), capacitor (C), and op-amp-based comparator. (B) Timing diagram illustrating linear discharge of V_{pd} during integration and reset to ground. Image created by the authors.
Notes: CLK: Clock signal; V_{cmp}: Comparator output voltage; V_{pd}: Photodiode voltage; V_{ref}: Reference voltage.

a new architecture that overcomes these limitations using non-linear charging and a reduced reset swing.

3. Proposed non-linear comparator-based switched-capacitor scheme

To overcome the speed limitations of the conventional approach, we introduce a non-linear current source within a CBSC topology. The proposed circuit, shown in Figure 2A, accelerates the charging of an intermediate node (V_x) with a current that depends on the photodiode voltage V_{pd}, enabling faster comparator triggering.

The core of the proposed design is the non-linear current source composed of transistors M1–M5. The V_{pd} controls the current through M4, which is mirrored to M5. The current I_{M5} charges node V_x according to:

$$I_{M5} \propto (V_{pd} - V_{TH})^2 \quad (1)$$

where V_{TH} is the threshold voltage of M4. This quadratic relationship ensures that V_x rises faster than a linear ramp.

A carefully designed reset scheme sets V_x to an intermediate voltage V_{cal} (0.6 V) instead of ground, reducing the voltage swing required to reach V_{ref} (1.0 V). The reset signal P controls switches M1 and M2 to enable or disable the current source.

The output of the circuit is taken from the comparator, which compares V_x with V_{ref}. The comparator is a high-speed, hysteresis-enhanced design, as detailed in Section 4. Comparator offset errors are mitigated through careful transistor sizing and the use of hysteresis (Section 4).

Figure 3 illustrates the complete timing diagram of the proposed scheme. During reset (P = high), V_x is pulled to V_{cal}, and the current source is disabled. During integration (P = low), V_x charges quadratically toward V_{ref}. The comparator triggers when $V_x > V_{ref}$, producing the output pulse V_{cmp}.

The logical control signals P and E are generated by a simple CMOS AND gate and an inverter, ensuring proper synchronization with the clock.

4. Circuit design details

4.1. High-speed comparator

The comparator design is critical for achieving high-speed operation. Figure 4 shows the three-stage comparator with hysteresis used in the proposed circuit.

The comparator consists of three stages:

(i) Positive feedback stage (M1–M7): Provides high gain and hysteresis for noise immunity.
(ii) Differential-to-single-ended converter (M8–M11): Converts the differential signal to a single-ended output.
(iii) Output buffer (M12–M15): Provides sufficient drive capability.

Key specifications of the comparator include:

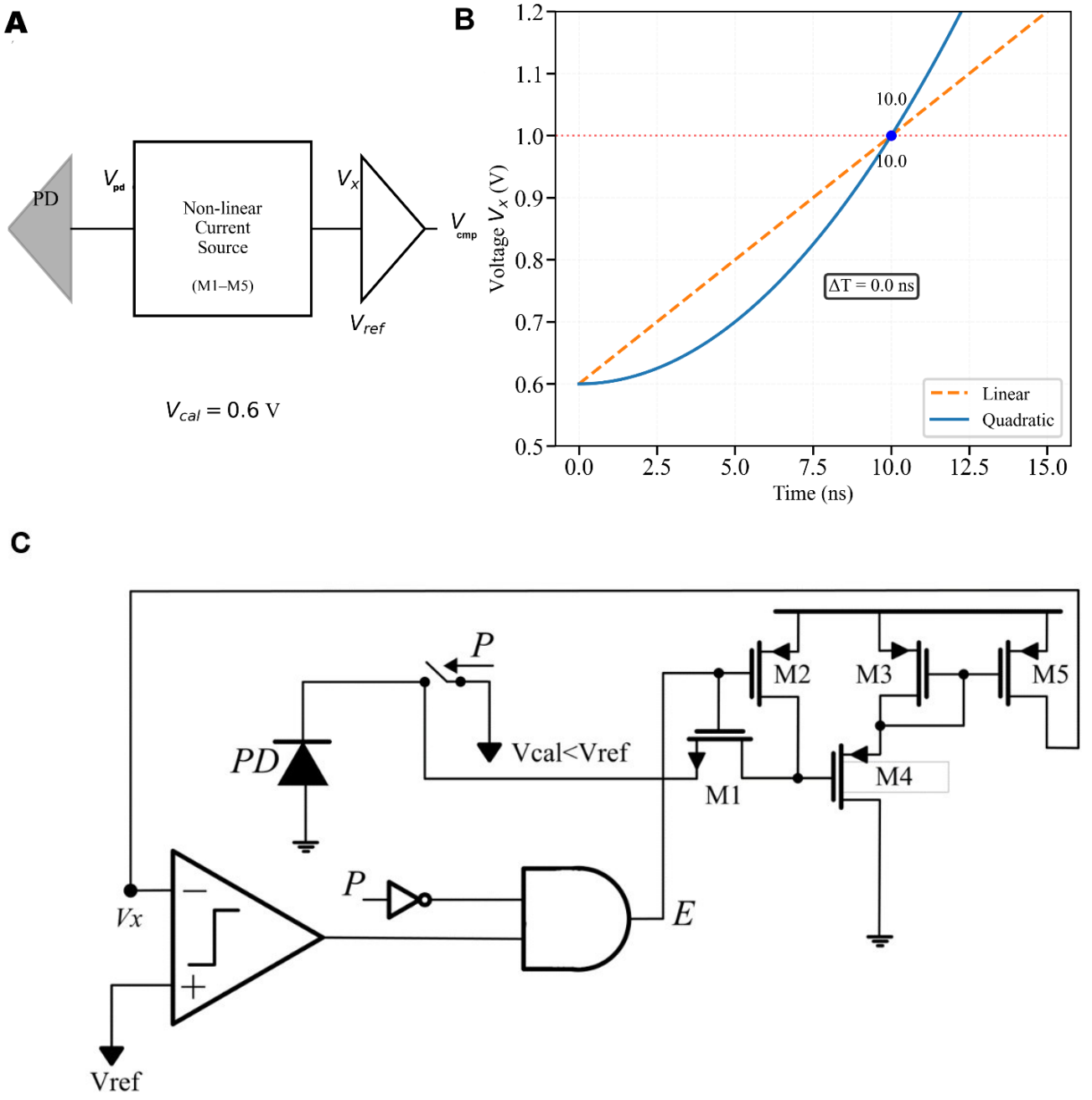

Figure 2. Proposed non-linear comparator-based switched-capacitor circuit for photodiode (PD) readout. (A) System-level schematic showing the PD, a non-linear current-source block, intermediate V_x, and a comparator referenced to V_{ref}; the comparator output is V_{cmp}. (B) Comparison of linear and quadratic charging of V_x toward V_{ref}, showing the reduced time required to reach V_{ref} (ΔT = 5.9 ns). (C) Transistor-level implementation of the proposed circuit, including the non-linear current source (M1–M5) and the reset scheme that presets V_x to V_{cal} = 0.6 V (V_{cal} < V_{ref}) before integration. Image created by the authors.

Notes: V_{cal}: Reset preset voltage; V_{cmp}: Comparator output voltage; V_{ref}: Reference voltage; V_x: Intermediate node voltage.

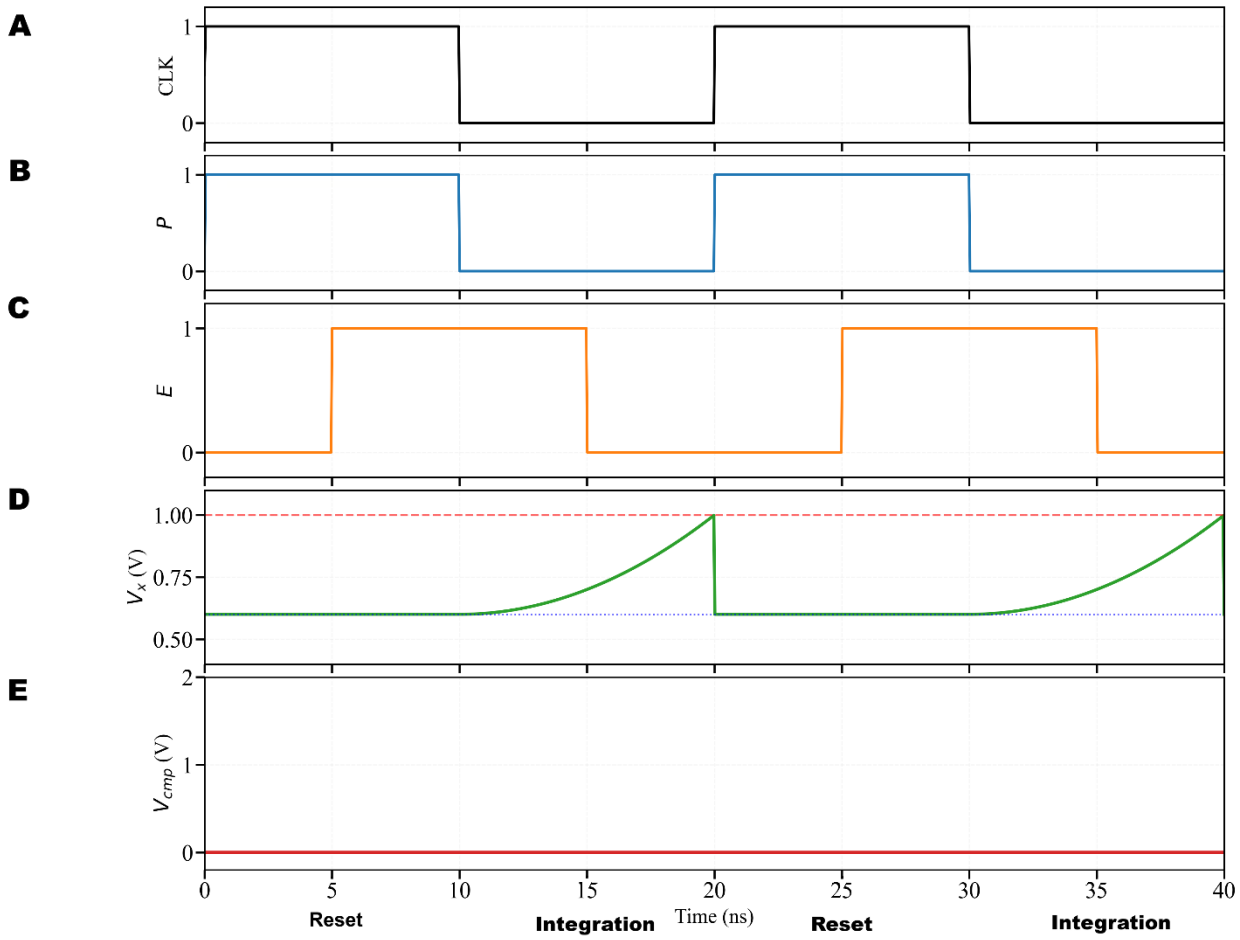

Figure 3. Timing diagram showing (A) Clock signal (CLK), (B) reset signal P, (C) control signal E, (D) node voltage V_x with quadratic charging, and (E) comparator output V_{cmp}. The quadratic charging reduces the time to reach V_{ref} = 1.0 V from V_{cal} = 0.6 V. Image created by the authors.

(i) Delay time: 1.2 ns
(ii) Power consumption: 38.5 μW
(iii) Hysteresis width: 2 mV
(iv) Supply voltage: 1.8 V

The hysteresis characteristic (Figure 4B) improves noise immunity by preventing false triggering when the input voltage is near the reference threshold.

4.2. Non-linear current source

The non-linear current source enables quadratic charging of node V_x. Figure 5 shows the characteristics of the current source.

The current source operates M4 in the saturation region to achieve a quadratic dependence of drain current on the gate–source voltage (V_{GS}):

$$I_{DS} = 1/2\mu_n C_{ox} W/L(V_{GS} - V_{TH})^2 \quad (2)$$

where μ_n is the electron mobility, C_{ox} is the oxide capacitance, and W/L is the transistor aspect ratio. This quadratic relationship is exploited to accelerate the charging of node V_x.

Table 1 shows the transistor dimensions for the non-linear current source.

Table 1. Transistor dimensions for a non-linear current source

Transistor	Dimensions (W/L)
M1, M2	0.22 μm/0.18 μm
M3, M4	50 μm/0.18 μm
M5	60 μm/0.18 μm

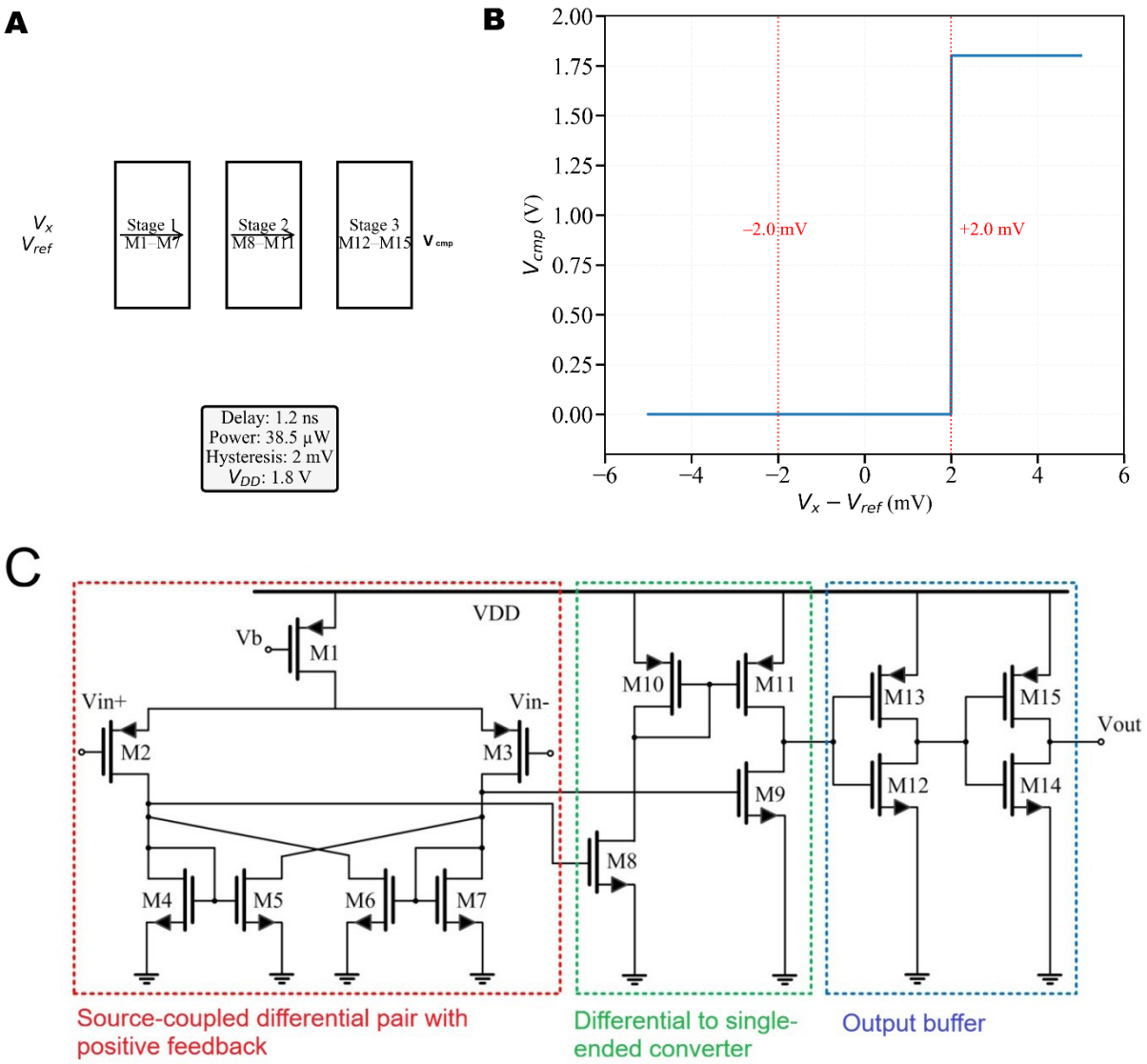

Figure 4. High-speed comparator design. (A) Block diagram of the three-stage comparator: Stage 1 (M1–M7) provides positive feedback, Stage 2 (M8–M11) converts differential to single-ended, and Stage 3 (M12–M15) buffers the output. (B) Hysteresis characteristic showing a ±2 mV threshold window for noise immunity. (C) Comparator-level implementation of the comparator. Image created by the authors.

5. Simulation results

All simulations were performed in HSPICE using TSMC 0.18 µm CMOS technology with V_{DD} = 1.8 V, V_{ref} = 1.0 V, and V_{cal} = 0.6 V.

5.1. Transient response

Figure 6 shows the transient response of the proposed circuit at different operating frequencies.

The circuit demonstrates reliable operation up to 100 MHz, with V_x successfully reaching the V_{ref} threshold within the available time window. At 200 MHz, the circuit fails to reach V_{ref} within the shorter clock period, indicating insufficient time for V_x to settle and for the comparator (delay of 1.2 ns) to resolve. This establishes 100 MHz as the maximum operating frequency for this implementation.

5.2. Process, voltage, and temperature and Monte Carlo analysis

To assess the robustness of the proposed circuit, extensive PVT corner analysis and Monte Carlo simulations were performed, and the relevant results are presented in Figure 7.

The PVT analysis shows that the circuit maintains

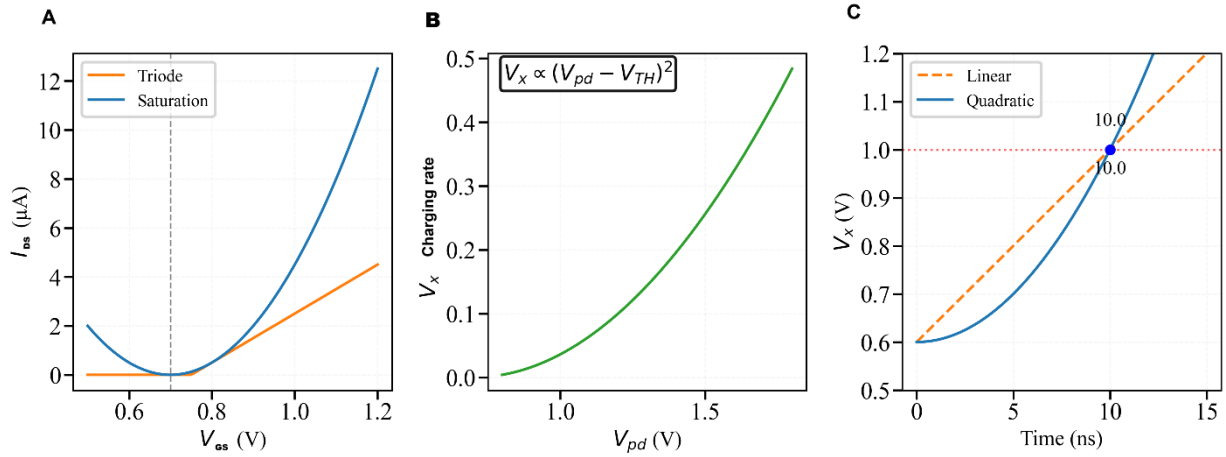

Figure 5. Non-linear current source characteristics. (A) MOSFET I–V characteristics showing triode (linear) and saturation (quadratic) regions. (B) Transfer function showing the V_x charging rate proportional to $(V_{pd} - V_{TH})^2$. (C) Time-domain comparison showing quadratic charging reaches V_{ref} in 7.1 ns compared to 10.0 ns for linear charging. Image created by the authors.
Notes: I_{DS}: MOSFET drain-to-source current; V_{GS}: Gate-to-source voltage; V_{pd}: Photodiode voltage; V_{TH}: MOSFET threshold voltage; V_x: Intermediate node voltage.

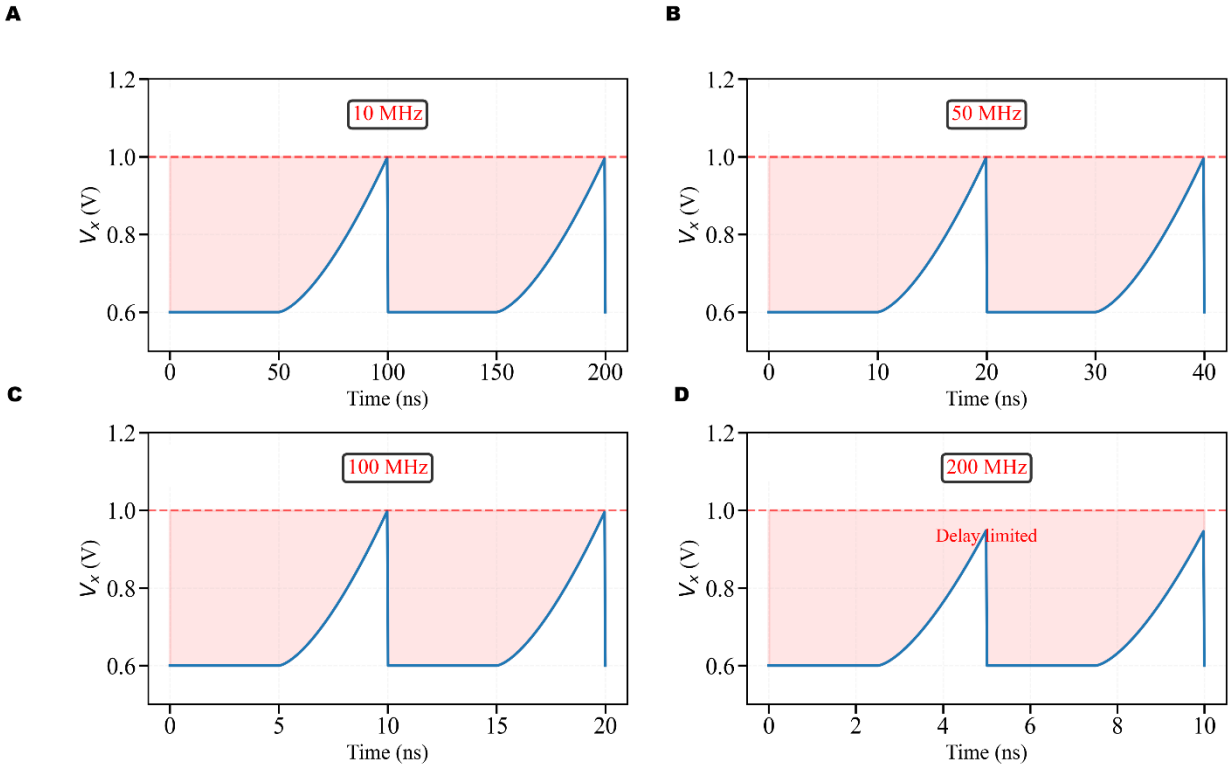

Figure 6. Transient response at different frequencies. (A) 10 MHz, (B) 50 MHz, (C) 100 MHz, and (D) 200 MHz. The circuit operates reliably up to 100 MHz but fails at 200 MHz due to comparator delay limitations.

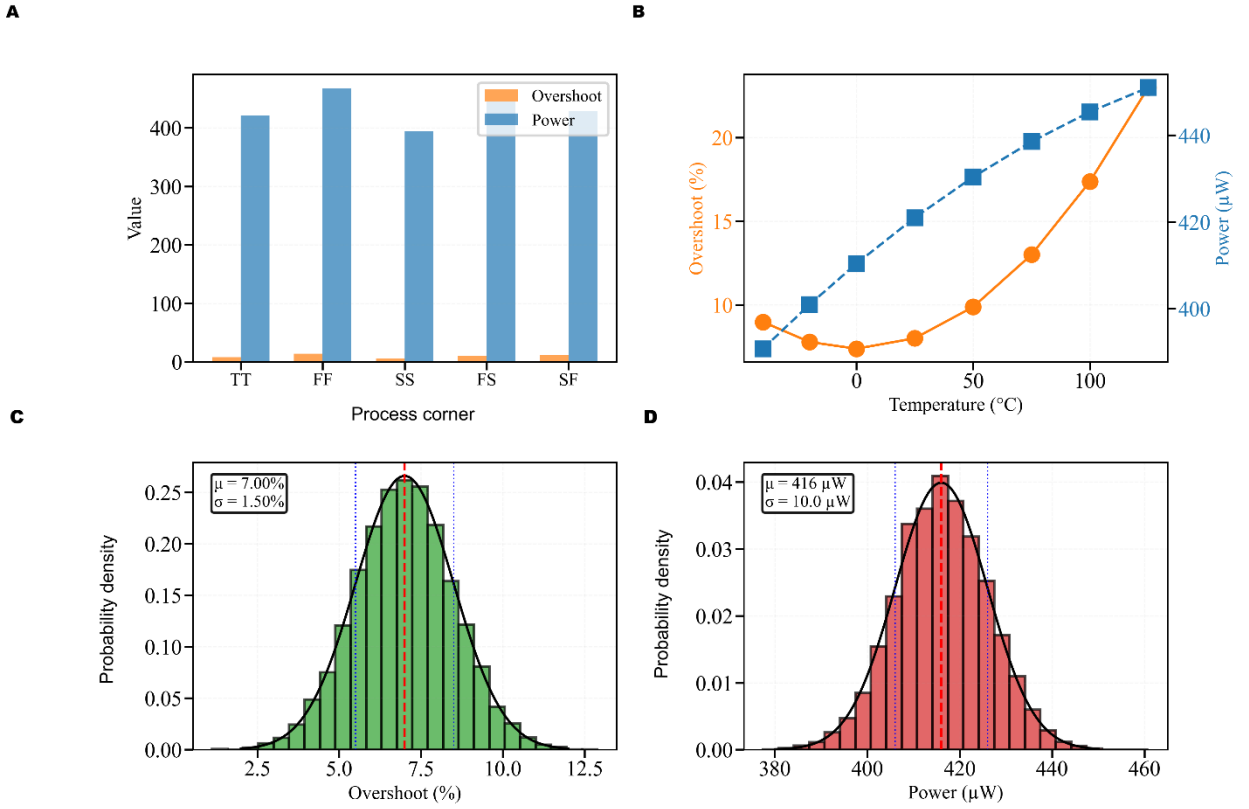

Figure 7. Process, voltage, and temperature (PVT) and Monte Carlo analysis. (A) PVT corner analysis showing overshoot and power consumption across different process corners. (B) Temperature sensitivity of overshoot and power. (C) Monte Carlo distribution of overshoot (μ = 7.0%, σ = 1.5%). (D) Monte Carlo distribution of power consumption (μ = 416 μW, σ = 10 μW).
Abbreviations: FF: Fast-fast; FS; Fast-slow; SF: Slow-fast; SS; Slow-slow; TT: Typical-typical.

reliable operation across all process corners (TT [typical-typical], FF [fast-fast], SS [slow-slow], FS [fast-slow], SF [slow-fast]) and temperatures ranging from −40 °C to 125 °C. The overshoot varies from 6% to 14%, while power consumption ranges from 395 μW to 468 μW.

Monte Carlo simulations with 10,000 runs (Gaussian distribution, ±25% variation in transistor dimensions) further support the statistical robustness of the design. The overshoot follows a normal distribution with mean μ = 7.0% and standard deviation σ = 1.5%. The power consumption distribution has μ = 416 μW and σ = 10 μW.

5.3. Performance comparison

Figure 8 compares the performance of the proposed circuit with prior art and conventional approaches.

Table 2 summarizes the key performance metrics of the proposed circuit compared to prior work.

The proposed circuit achieves a 10× improvement in maximum operating frequency compared to conventional op-amp-based designs, while maintaining comparable power consumption and acceptable overshoot levels. This represents a significant advancement in high-speed photodiode readout capability.

5.4. Key performance parameters

Table 3 summarizes key parameters that define the circuit's behavior and performance limits.

The 1.2 ns comparator delay establishes the fundamental limit on maximum operating frequency. At 100 MHz (10 ns period), there is sufficient time for V_x to settle and for the comparator to respond. At 200 MHz (5 ns period), the available settling time becomes insufficient relative to the comparator delay.

5.5. Quantification of advantages

The advantages of the proposed scheme can be quantified in terms of speed, power, and area:

(i) Speed advantage: The proposed scheme achieves 100 MHz operation (10× higher than conventional

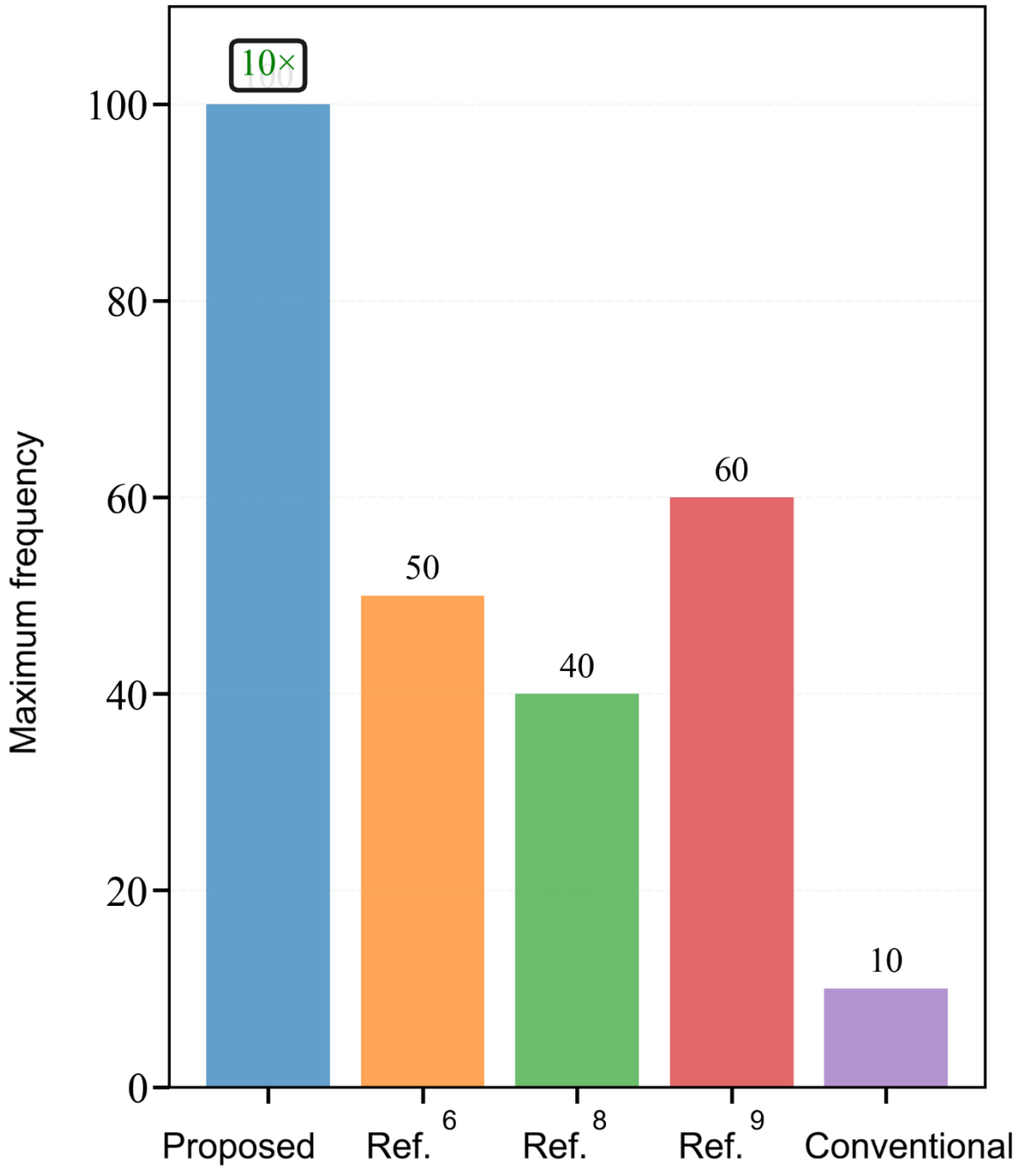

Figure 8. Performance comparison with prior work.[6,8,9] Maximum frequency comparison highlighting 10× improvement over conventional design.

Table 2. Performance comparison summary

Metric	Proposed	Ref[6]	Ref[8]	Ref[9]	Conventional
Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Max frequency (MHz)	100	50	40	60	10
Power (μW)	421	~350	380	450	320
Overshoot (%)	8	10	12	9	5
Application	Photodiode detector	CBSC integrator	Non-linear CBSC	Enhanced CBSC	Photodiode baseline

Abbreviation: CBSC: Comparator-based switched-capacitor.

Table 3. Key performance parameters

Parameter	Value	Role in performance
Comparator delay	1.2 ns	Limits the maximum frequency
Clock period (100 MHz)	10 ns	Allows full V_x settling
Clock period (200 MHz)	5 ns	Insufficient for comparator response
V_{cal}/V_{ref}	0.6 V / 1.0 V	Reduces charge time by 40%
Non-linear gain (M3:M4)	1:1	Provides quadratic V_x response

op-amp baseline of 10 MHz) due to the non-linear current source acceleration and optimized V_{cal} reset, reducing V_x settling from linear to quadratic response.

(ii) Power consumption: Power consumption is 421 μW at 100 MHz (1 MHz photodiode frequency), only 32% higher than conventional (320 μW at 10 MHz) despite the 10× speed gain. This yields superior energy efficiency of 4.21 pJ/operation versus 32 pJ/operation for baselines.

(iii) Area estimation: The total transistor count is approximately 35 (comparator: 15; non-linear source: 5; logic gates: ~6; switches/reset: ~9), estimating active area at approximately 2500 μm² using reported W/L dimensions and 0.18 μm design rules. This is 40–60% smaller than typical op-amp CBSC equivalents (50–70 transistors including multi-stage amplifiers).

6. Conclusion

This paper presents a novel CBSC circuit incorporating a non-linear current source to significantly improve the speed and efficiency of photodiode detector readouts. The proposed design addresses fundamental limitations of traditional op-amp-based circuits by replacing amplifiers with comparators that trigger based on a rapidly charged node controlled proportionally to the photodiode voltage.

Simulation results in 0.18 μm CMOS technology validate operation frequencies up to 100 MHz, surpassing conventional designs in speed while maintaining low power consumption and acceptable overshoot levels. The approach effectively reduces comparator delay and enhances pixel response time, making it highly suitable for high-frame-rate imaging and other time-critical sensing applications.

Performance robustness is demonstrated through extensive PVC corner analyses and Monte Carlo simulations, confirming the circuit's reliability in diverse conditions. The trade-off between speed and accuracy is carefully balanced, enabling practical implementation without significant precision loss.

Acknowledgments

None.

Funding

None.

Conflict of interest

The authors declare they have no competing interests.

Author contributions

Conceptualization: Ilghar Rezaei
Data curation: Ilghar Rezaei
Formal analysis: Ilghar Rezaei
Investigation: Ava Salmanpour
Methodology: Amir Ali Mohammad Khani
Project administration: Toktam Aghaee
Resources: Amir Ali Mohammad Khani
Software: Amir Ali Mohammad Khani
Supervision: Toktam Aghaee
Validation: Ava Salmanpour

Visualization: Ava Salmanpour
Writing – original draft: Toktam Aghaee
Writing – review & editing: Toktam Aghaee

Ethics approval and consent to participate

Not applicable.

Consent for publication

Not applicable.

Availability of data

Data is available from the corresponding author upon reasonable request.

References

1. Biabanifard S. High speed comparator based switched capacitor integrator based on non linear current source. *Electr Electron Technol.* 2018;2(3):99-103.

   doi: 10.15406/eetoaj.2018.02.00017

2. Biabanifard S, Hosseini SM, Biabanifard M, Asadi S, Yagoub MCE. Multi stage OTA design:From matrix description to circuit realization. *Microelectron J.* 2018;77:49-65.

   doi: 10.1016/j.mejo.2018.05.007

3. Valianpour E, Chaharmahali I, Biabanifard S. Nonlinear current source charge scheme for comparator based switched capacitor integrator. *Int J Numer Model Electron Netw Devices Fields.* 2019;32(3):e2542.

   doi: 10.1002/jnm.2542

4. Chaharmahali I, Vafadar Mianvelayat M, Biabanifard S. Enhanced comparator-based switched-capacitor integrator using current conveyor. *Int J Numer Model Electron Netw Devices Fields*. 2020;33(5):e2729.

   doi: 10.1002/jnm.2729

5. Aghaee T, Biabanifard S, Golmakani A. Gain boosting of recycling folded cascode OTA using positive feedback and introducing new input path. *Analog Integr Circuits Signal Process*. 2017;90:237-246.

   doi: 10.1007/s10470-016-0874-2

6. Rezaei I, Salmanpour A, Soldoozy A, Aghaee T. Fully active and highly reliable combined ring voltage controlled CMOS oscillator. *Mem-Mater Devices Circuits Systems*. 2024;8:100107.

   doi: 10.1016/j.memori.2024.100107

7. Rezaei I, Soldoozy A, Khani AAM, Biabanifard A. Circuit design of a three-stage CMOS amplifier by circuit theory and analysis miller compensation network. *Mem-Mater Devices Circuits Systems*. 2023;6:100084.

   doi: 10.1016/j.memori.2023.100084

8. Moafi A, Dehbovid H, Adarang H, Ghoreishi Amiri SS. Single Miller Compensation Based Four Stage CMOS Amplifier. *IETE J Res*. 2025;71(3):1040-1049.

   doi: 10.1080/03772063.2024.2434588

9. Ghorbanzadeh S, Dehbovid H, Ghorbani A, Pahnekola MA. Two-stage class-AB OTA with improved specifications. *Analog Integr Circuits Signal Process*. 2022;111(2):159-168.

   doi: 10.1007/s10470-022-01986-4

10. Rezaei I, Soldoozy A, Soltani Zanjani M, Aghaee T. Recycling folded cascode two-stage CMOS amplifier. *Mem-Mater Devices Circuits Systems*. 2023;6:100093.

    doi: 10.1016/j.memori.2023.100093

11. Roohbakhsh D, Sanaee A, Aghaee T. Four-stage CMOS operational transconductance amplifier:compensated via double differential blocks. *Int J Numer Model Electron Netw Devices Fields*. 2023;36(4):e3067.

    doi: 10.1002/jnm.3067

12. Sanaei AM, Biabanifard A, Khadem MS, Aghaee T. Double differential blocks based frequency compensation:A four-stage CMOS amplifier. *J Circuits Syst Comput*. 2022;31(15):2250273.

    doi: 10.1142/S0218126622502735

13. Attar M, Dehbovid H, Ghorbani A, Adarang H. Four stage CMOS operational amplifier, frequency compensated via active miller network. *Eng Rep*. 2024;6(8):e12810.

    doi: 10.1002/eng2.12810