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Engineering Science in Additive Manufacturing

PERSPECTIVE ARTICLE

Why semiconductor additive manufacturing is challenging—and what comes next

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Abstract

Semiconductors underpin modern electronics, optoelectronics, sensing, and energy technologies, yet their manufacturing remains dominated by centralized, tool-intensive, and largely planar process flows. Additive manufacturing (AM) offers a complementary pathway that can reduce material waste, accelerate prototyping, and unlock three-dimensional (3D) semiconductor architectures that are difficult to realize using conventional fabrication. However, AM of semiconductors is still in its infancy and has been demonstrated for only a limited set of materials and processes. This perspective synthesizes the current landscape of semiconductor AM by compiling reported 3D-printable semiconductor systems and mapping them to the corresponding AM techniques, including laser powder bed fusion, selective laser sintering, gas-phase reactive AM, inkjet printing, electrohydrodynamic redox printing, two-photon lithography, aerosol jet printing, extrusion-based AM, and laser-directed energy deposition. The key process-specific barriers are critically discussed—spanning feedstock limitations, densification and cracking, stoichiometry control and volatilization, texture and compositional heterogeneity, post-processing burdens, contamination, and scalability. On this basis, a length-scale–guided roadmap is proposed: laser powder bed fusion is positioned as the most promising route for cm–mm thermoelectric architectures, with advances in substrate/feedstock design, atmosphere control, and microstructure/defect engineering; ink-based and reactive approaches are highlighted for sub-mm to micro-scale functional devices through improved ink chemistry, 3D buildup, and multi-material integration; and electrohydrodynamic redox printing/two-photon lithography are identified as leading candidates for sub-micron to nanoscale fabrication, where material diversification, low-temperature conversion, residue mitigation, and hybrid integration with conventional microfabrication are essential. Collectively, this perspective clarifies terminology, consolidates the emerging evidence base, and outlines research priorities required to transition semiconductor AM from proof-of-concept demonstrations toward robust, application-relevant device manufacturing.

Keywords: Additive manufacturing; Three-dimensional printing; Semiconductor; Laser powder bed fusion; Ink-based printing; Two-photon lithography

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Citation: Ghasemi A, Sing SL. Why semiconductor additive manufacturing is challenging—and what comes next. *Eng Sci Add Manuf.* 2026;2(1):026060003. doi: 10.36922/ESAM026060003

Received: February 7, 2026

Revised: February 26, 2026

Accepted: February 28, 2026

Published online: March 26, 2026

1. Introduction

Semiconductors are a broad family of materials that form the technological backbone of modern society. They are embedded in nearly every aspect of daily life, enabling devices and systems that individuals rely on routinely, often without noticing their presence. From everyday consumer products such as smartphones, smart televisions, wearable devices, and household appliances to more advanced technologies—including cloud computing infrastructure, navigation systems, and space technologies—semiconductors play a central role in shaping how information is processed, communicated, and utilized. Their widespread integration across consumer, industrial, and digital platforms underscores their fundamental importance to modern life.[1,2]

From an electrical conductivity perspective, materials are commonly classified into conductors, semiconductors, and insulators, with semiconductors occupying an intermediate position between the other two classes.[3] This distinction can be understood in terms of the valence and conduction bands (Figure 1A), separated by an energy gap that governs electrical behavior. In conductors, these bands overlap, enabling free electron movement and high conductivity. In insulators, a large band gap suppresses carrier excitation. Semiconductors possess a finite but smaller band gap, allowing electrons to be thermally, optically, or electrically excited into the conduction band, generating electron–hole pairs and enabling controlled charge transport.[4]

An intuitive way to visualize this behavior is to imagine two floors in a building: in conductors, the floors are connected by an open staircase, allowing people to move freely, while in insulators, the floors are separated by a high wall. Semiconductors lie between conductors and insulators, where a short staircase is present, enabling movement only when sufficient energy is provided. It is worth noting that in practical situations, the energy bands in semiconductors may locally shift or bend in response to external electric fields, interfaces, or charge accumulation, thereby modifying how easily charge carriers are generated and transported near surfaces or junctions.[5]

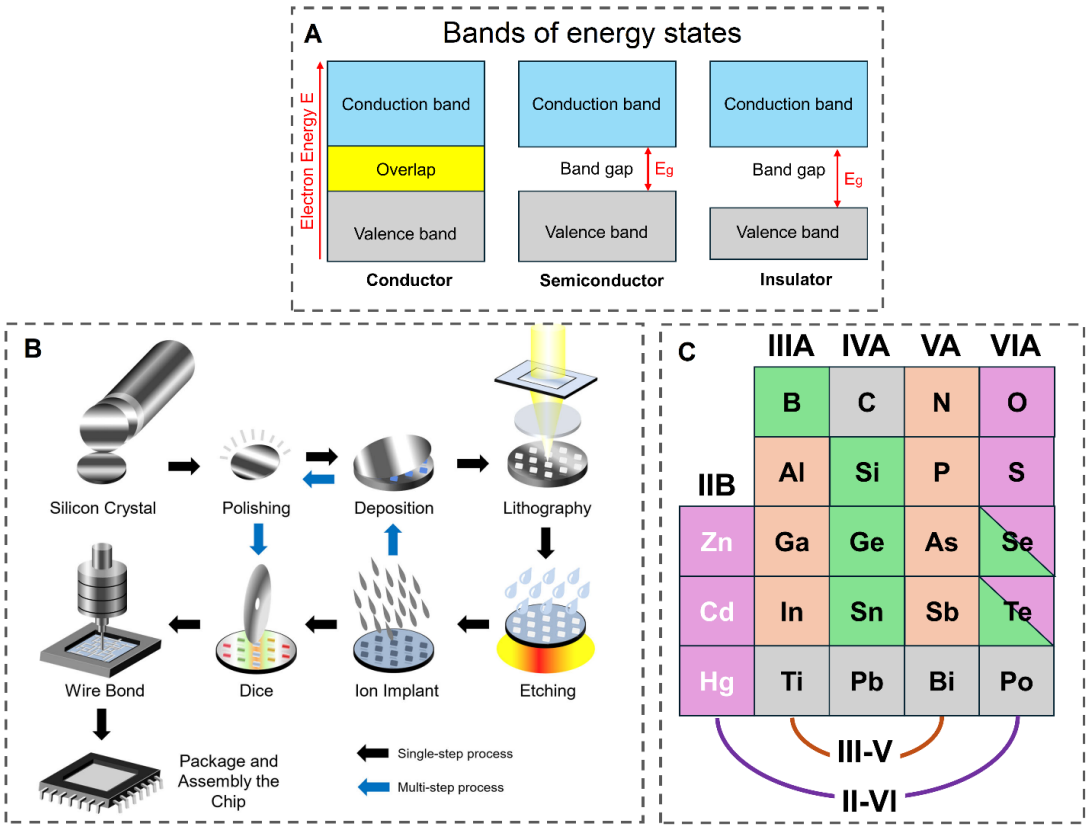

Figure 1. Overview of semiconductor fundamentals and conventional semiconductor manufacturing concepts. (A) Schematic comparison of electronic band structures in conductors, semiconductors, and insulators (created by the authors). (B) Simplified overview of conventional semiconductor manufacturing, from single-crystal growth and wafer processing to device fabrication and chip packaging (reproduced from Ref.[6]). (C) Simplified periodic table highlighting elemental groups relevant to compound semiconductor families (created by the authors).

The electrical properties of semiconductors can be tailored through doping, that is, the controlled introduction of trace impurity elements. Donor dopants increase free electron concentration (*n*-type), whereas acceptor dopants generate holes (*p*-type).[3] Rather than altering the fundamental band structure, doping introduces energy states that facilitate carrier excitation and enhance electrical conductivity. An intuitive way to visualize this effect is to imagine a city with bridges connecting two neighborhoods: adding dopants is similar to constructing shorter access roads that allow people to move between neighborhoods more easily, although the neighborhoods themselves remain in the same locations. Through controlled doping, the electrical response of semiconductors can be precisely tailored for a wide range of electronic, optoelectronic, and energy-related applications.

From a materials-chemistry perspective, semiconductor materials may be broadly classified into (i) elemental semiconductors (e.g., silicon [Si] and germanium); (ii) compound semiconductors, including III–V, II–VI, and IV–IV systems (e.g., gallium arsenide and zinc oxide [ZnO]); (iii) metal-oxide semiconductors (e.g., titanium dioxide [TiO_2] and stannic oxide); (iv) chalcogenide semiconductors (e.g., molybdenum disulfide and bismuth telluride); (v) organic semiconductors (e.g., pentacene and poly[3-hexylthiophene]); perovskite semiconductors (e.g., methylammonium lead iodide and cesium lead bromide); (vi) wide- and ultra-wide-band gap semiconductors (e.g., silicon carbide and gallium nitride [GaN]); and (vii) emerging semiconductor systems (e.g., two-dimensional materials and topological semiconductors).[1,7-16] Here, the Roman numerals in the III–V, II–VI, and IV–IV designations denote the corresponding column numbers of the constituent elements in the periodic table (Figure 1C), indicating the periodic-group elemental combinations that form these compound semiconductor families. These semiconductors underpin a wide range of technologies, including electronics, optoelectronics, photovoltaics, thermoelectrics (TEs), sensing, power conversion, quantum technologies, bioelectronics, radiation detection, and integrated photonics.[17]

Conventional semiconductor manufacturing is based on a sequence of highly controlled and well-established processing steps that have been refined over several decades to achieve the precision, reliability, and scalability required for modern electronic and optoelectronic devices. These conventional approaches, as shown in Figure 1B, rely on centralized fabrication facilities, sophisticated equipment, and multi-stage workflows to transform high-purity semiconductor materials into functional components using the following[18]:

(a) Crystal growth

The manufacturing process begins with the production of high-purity single-crystal semiconductor ingots, most commonly Si, which serve as the starting material for wafer fabrication. Si crystals are typically grown using the Czochralski crystal growth method, in which a seed crystal is drawn from molten Si under controlled thermal and rotational conditions to obtain a large, defect-minimized single crystal. Compound semiconductors may employ alternative crystal growth techniques.

(b) Wafer fabrication

The grown ingots are sliced into thin, circular wafers using precision cutting tools and subsequently polished to achieve ultra-smooth, mirror-like surfaces. Wafer thickness and surface quality are critical parameters that influence mechanical stability and downstream processing.

(c) Doping and carrier concentration control

Electrical properties are tailored by introducing controlled amounts of impurity atoms to create *n*-type or *p*-type regions within the semiconductor. Ion implantation is the predominant modern technique, offering high spatial accuracy and repeatability compared to earlier diffusion-based approaches.

(d) Photolithographic patterning

Geometric features are defined by transferring patterns from photomasks onto photosensitive resist layers deposited on the wafer surface. This step establishes the spatial arrangement and functional regions of semiconductor devices.

(e) Etching and material removal

Exposed regions of the wafer are selectively removed using chemical or plasma-based etching processes, enabling the formation of micro- and nanoscale device features.

(f) Oxide formation and surface passivation

Thin oxide layers are formed on the wafer surface to provide electrical insulation, chemical protection, and interface control. These layers are commonly produced through thermally activated or vapor-phase processes.

(g) Thin-film deposition

Additional conductive and insulating layers are deposited using techniques such as sputtering or chemical vapor deposition, allowing the construction of multilayer device architectures.

(h) Metallization and interconnection

Metal contacts and interconnects are formed to electrically link the semiconductor structures to external circuitry, completing the fabrication of functional semiconductor devices.

Despite remarkable advances in conventional semiconductor manufacturing—particularly in achieving nanoscale dimensional accuracy, high reproducibility, and efficient large-scale production—these approaches suffer from several inherent limitations. First, the highly optimized and tool-intensive nature of conventional fabrication workflows makes rapid prototyping and exploratory design iteration challenging, thereby slowing early-stage scientific discovery and technology development.[19] Second, conventional processes are often costly and time-consuming for customized or small-batch production, as design changes typically require new masks, tooling, or equipment reconfiguration, which is economically inefficient for personalized or application-specific electronics.[20] Third, semiconductor manufacturing relies heavily on hazardous chemicals and complex chemical processing steps, such as etching and cleaning, raising concerns related to worker safety, environmental impact, and waste disposal.[18]

In addition, while three-dimensional (3D) semiconductors and metal-oxide architectures have been shown to offer substantial performance enhancements, traditional fabrication techniques are largely restricted to planar or quasi-two–dimensional (2D) geometries, limiting access to fully 3D device designs.[21,22] This constraint is further compounded by the limited geometric flexibility of conventional methods, which favor relatively simple and repetitive layouts.[23] Finally, the subtractive nature of many fabrication steps leads to significant material waste, particularly during cutting and etching, thereby reducing overall material efficiency and sustainability.[24,25]

Additive manufacturing (AM), also known as 3D printing, has been proposed as a promising approach to address many of the limitations associated with conventional semiconductor manufacturing and to meet emerging technological demands. AM is widely regarded as a disruptive manufacturing paradigm that has already transformed several industries, with successful real-world adoption in sectors such as aerospace, automotive, tooling and die manufacturing, and turbine engineering.[26-29] Compared to subtractive manufacturing, AM offers a combination of compelling advantages, including a high buy-to-fly ratio that improves material efficiency and sustainability, reduced material waste and associated carbon dioxide emissions, and unparalleled geometric freedom.[28,30] Moreover, AM typically requires minimal or no tooling and molds, enabling rapid design iteration, cost-effective customization, and near-net-shape fabrication with limited post-processing.[31-33] The inherently layer-wise nature of AM further provides access to novel microstructures, functionally optimized architectures, and 3D designs that enable performance-driven components, which are difficult or impractical to realize using conventional manufacturing routes.

According to the International Organization for Standardization (ISO)/American Society for Testing and Materials (ASTM) 52900[34], AM is defined as "a process of joining materials to make parts from 3D model data, usually layer upon layer, as opposed to subtractive manufacturing and formative manufacturing methodologies." This standard classifies AM technologies into seven process categories: vat photopolymerization, material extrusion, material jetting, binder jetting, powder bed fusion (PBF), directed energy deposition, and sheet lamination. The capability of these AM approaches to fabricate polymeric, metallic, alloy, composite, and ceramic components has been extensively investigated and well documented in the literature. In contrast, semiconductors have received comparatively limited attention within the context of AM, despite their central role in modern technologies. This perspective article seeks to place AM of semiconductors under focused scrutiny by critically examining the current state of the art, identifying key technical and material limitations, and outlining future research directions needed to advance this emerging field.

For clarity and consistency, the term "additive manufacturing" is used in this article to describe fabrication processes that satisfy the following criteria: (i) material is added in a layer-by-layer manner; (ii) the process enables the construction of 3D objects with material buildup along the build (Z) direction; and (iii) 3D objects are built directly from a digital data file. Processes meeting these three requirements are referred to as AM in this work, regardless of whether they fall within the current ISO/ASTM classification framework or represent newly developed or emerging techniques. It is also important to note that, within the semiconductor literature, terms such as "printing" and "additive" are frequently used outside the strict context of AM, which can be a source of confusion for scholars in the field of AM. In many cases, these terms refer to 2D coating, deposition, or patterning processes, rather than true 3D fabrication. For example, multi-photon lithography is used to deposit planar semiconductor films or patterns on substrates[35]; however, when such a process is employed solely to produce thin films without volumetric buildup in the Z direction, it does not satisfy the criterion of 3D object formation and therefore should not be classified as AM technology. Such processes, while additive in nature, do not involve volumetric buildup and therefore should not be classified as AM technologies. In other words, all AM processes are additive, but not all additive or deposition-based processes qualify as AM.

Table 1. Summary of semiconductor materials fabricated by powder-bed laser additive manufacturing processes

Process	Material	Laser power (W)	Scan speed (mm/s)	Hatch spacing (mm)	Powder layer thickness (mm)	Maximum relative density (%)	Remarks	References
L-PBF	Sb_2Te_3	60, 100	200, 300	0.05	2	99.91	Mixed elemental Sb and Te powders were directly blended and deposited as a non-conventional 2 mm-thick powder layer on a stainless-steel substrate. Each layer was selectively laser-melted twice to enhance densification. The process was designed to fabricate dense thermoelectric ingots rather than thin-layer AM builds. Laser processing was carried out under high-purity Ar (1.5–2.0 KPa). A commercial continuous fiber-laser with a wavelength of 1,064 nm was used	24
	Bi_2Te_3	25	500	0.0375	0.15	88	Pre-alloyed Bi_2Te_3 powder was manually spread and flattened inside a thin stainless-steel ring acting as a powder-bed container, and the process was repeated for eight layers. Printing was conducted under an N_2 atmosphere with O_2 <4% to limit oxidation. The utilized laser was a 1,070 nm diode-pumped ytterbium fiber laser, operating in continuous wave mode	36
	$Bi_2Se_{0.3}Te_{2.7}$	25	NA	0.0375	0.15	77	Commercial melt-grown $Bi_2Se_{0.3}Te_{2.7}$ ingots were ball-milled and sieved to particle sizes below 75 μm. Powder layers were manually deposited and flattened using a stainless-steel roller, and L-PBF was carried out under an Ar atmosphere with O_2 <1%. A continuous YAG laser with a 1,070 nm wavelength was used for printing	37
	$Bi_{0.4}Sb_{1.6}Te_3$	NA	NA	NA	0.05	NA	Highly pure elemental Bi, Sb, and Te powders were first reacted via thermal explosion synthesis, followed by ball milling of the porous ingot to produce pre-alloyed powder (<400 mesh). The powder was dispersed in alcohol to form a slurry, spread onto the substrate, and dried prior to printing. A composition-matched spark-plasma-sintered substrate was used, and all printing was performed under a high-purity 95% Ar, 5% H_2 (0.5 atm) protective atmosphere to prevent oxidation. A commercial fiber laser with a wavelength of 1,064 nm was utilized for part fabrication	38
	$Bi_2Te_{2.7}Se_{0.3}$	1–13	NA	NA	0.05	NA	Elemental Bi, Te, and Se powders were mixed according to stoichiometry and dispersed in alcohol to form a slurry. During laser scanning, SHS occurred in situ, converting the elemental mixture into the thermoelectric compound. Printing was conducted under a mixed Ar/H_2 protective atmosphere. A commercial fiber laser with a wavelength of 1,064 nm was utilized for part fabrication	39
	$Bi_2Te_{2.7}Se_{0.3}$	3–10	50–500	0.05	0.03	NA	$Bi_2Te_{2.7}Se_{0.3}$ ingots were first synthesized by SHS, then ball-milled to produce pre-alloyed powder. The powder was mixed with alcohol to form a slurry and uniformly deposited onto the substrate prior to L-PBF. Printing was carried out under an Ar atmosphere at 0.5 atm. A commercial fiber laser with a wavelength of 1,064 nm was utilized for part fabrication	40

(*Cont'd...*)

doi: 10.36922/ESAM026060003

Table 1. *Continued*

Process	Material	Laser power (W)	Scan speed (mm/s)	Hatch spacing (mm)	Powder layer thickness (mm)	Maximum relative density (%)	Remarks	References
L-PBF	$Si_{80}Ge_{20}$	99–142	300–600	0.045	0.03	97.8	Pre-alloyed $Si_{80}Ge_{20}$ gas-atomized powder was printed directly onto an 430 stainless-steel substrate. To promote heat dissipation and improve densification, the laser jump speed between adjacent tracks was significantly reduced, and a unidirectional scan strategy was employed. Despite achieving high relative density, cracking was observed in all samples. Printing was carried out under an Ar atmosphere with O_2<1,000 ppm. A laser beam with a wavelength of 1,064 nm was utilized in this study (the laser source is not reported)	41
	$Si_{50}Ge_{50}$/ $Si_{80}Ge_{20}$	25–75	25–500	0.0375, 0.05	0.2	59	Pre-alloyed $Si_{50}Ge_{50}$ and $Si_{80}Ge_{20}$ materials were ball-milled from bulk granules and sieved to particle sizes below 75 μm. To avoid fusion with the substrate, the first powder layer thickness was increased to 400 μm, followed by rescanning using identical or modified parameters. In some cases, powders were HF-washed to remove surface SiO_2 prior to printing. Prior to laser processing, the enclosure was purged with Ar until an oxygen sensor sensed O_2<100 ppm. A continuous wave Nd-YAG laser with a wavelength of 1,070 nm was used in this study	42
	$Bi_2Te_{2.7}Se_{0.3}$	6	80	0.05	0.09	96	SHS-synthesized $Bi_2Te_{2.7}Se_{0.3}$ ingots were ball-milled and processed into an aqueous slurry. A dispenser-printing system was used to deposit uniform powder layers prior to L-PBF, with an optimized droplet spacing of 350 μm. This hybrid approach aimed at improving powder-bed quality. All experiments were carried out under a high-purity Ar atmosphere of 0.5 atm. A commercial fiber laser with a 1,064 nm wavelength was utilized for printing	43
	CP Si	80–100	300–1,800	0.09	0.03	98.5	Elemental silicon powders with purities of 99.61% and 99.87% were directly processed by L-PBF on a 316L stainless-steel substrate. High relative density was achieved, although cracking remained a concern. A high-purity Ar gas was flushed continuously inside the process chamber to minimize/avoid any possible oxidation. Nd: YAG laser was used for printing (the wavelength is not reported)	44
SLS	$Bi_{0.5}Sb_{1.5}Te_3$	30	3,200	0.05, 0.08	0.05	54	Pre-alloyed $Bi_{0.5}Sb_{1.5}Te_3$ powders were produced by ball milling bulk alloy ingots (100 mesh) and processed using a CO_2 laser (10.6 μm wavelength). Porous structures were intentionally fabricated to reduce thermal conductivity while maintaining acceptable electrical performance and mechanical strength	45

Abbreviations: AM: Additive manufacturing; Ar: Argon; Bi: Bismuth; CP: Commercially pure; Ge: Germanium; HF: Hydrofluoric acid; L-PBD: Laser powder bed fusion; NA: Not available; Nd-YAG: Neodymium-doped yttrium aluminum garnet; Sb: Antimony; Se: Selenium; SHS: Self-propagating high-temperature synthesis; Si: Silicon; Te: Tellurium; YAG: Yttrium aluminum garnet.

Table 2. Summary of semiconductor materials fabricated by other additive manufacturing techniques

Process	Material	3D-printing feedstock and process variables	Post-processing	References
GRAM	GaN	Liquid Ga was deposited from a molten Ga bath as a liquid-phase precursor onto *c*-plane sapphire substrates, followed by reactive conversion to GaN in a chamber under flowing N_2/NH_3 gas mixtures. Crystallization was carried out at 1,050 °C for 5–30 min, with N_2:NH_3 ratios between 1.25 and 50 controlled via NH_3 flow rate	NA	46
	GaN	Liquid Ga was deposited onto 2-inch *c*-plane sapphire wafers and subsequently crystallized to GaN in a vacuum chamber under flowing inert carrier gas and NH_3 (99.99%). Growth was conducted at 1,000 °C and 68–72 Torr, with delayed NH_3 introduction (0–10 min) and maintained during cooling to ensure N_2 overpressure	Wet etching was applied after each Ga deposition step to remove native Ga_2O_3 prior to subsequent growth	47
IJP	ZnO	A solid–gel zinc acetate ink (0.05 M in ethanol) was inkjet-printed onto Kapton® polyimide substrates using 10 pL droplets, a 10 μm drop spacing, and 10 print passes, with substrate temperatures of 40–60 °C	Immediately after printing, films were heated at 200 °C for 10 min to decompose the precursor, followed by furnace annealing at 400 °C for 1 h to sinter ZnO while preserving substrate integrity	48
	ZnO	A 50 mM zinc acetate–ethanol ink was inkjet-printed onto Si/SiO_2 substrates	The printed precursor layer was thermally decomposed on a hotplate at 200 °C for 10 min to form polycrystalline ZnO, followed by post-annealing in a quartz tube furnace at 250–350 °C for 30 min to further improve film quality	49
EHD-RP	Zn/ZnO	Zn was electrohydrodynamically printed using etched Zn wire anodes onto Au/Ti-coated Si substrates, with typical voltages of 110–130 V and a nozzle–substrate distance of 5–10 μm. Printing was conducted under an Ar atmosphere (<100 ppm O_2)	Post-print oxidation was performed by annealing at 325 °C for 6 h in air, converting deposited Zn to ZnO	50
TPL	ZnO	ZnO microstructures were fabricated using a zinc-ion–containing aqueous photoresin based on zinc nitrate, PEGDA, and DETC photoinitiator. Structures were written at 50 mW laser power and 1 mm/s scan speed on glass substrates with silicon chips as writing interfaces	Printed structures were calcined in air at 500 °C with controlled heating and cooling rates to form ZnO	23
AJP	ZnO	Water-based binder-free ZnO nanoparticle inks, including hybrid ZnO–TiO_2–Al_2O_3 dispersions, were deposited onto alumina substrates via ultrasonic AJP using a 150 μm nozzle and N_2 carrier/sheath gases, with platen temperatures up to 100 °C for in situ drying	Printed structures were densified by thermal sintering at 950 °C for 6 h	20
EAM	TiO_2	TiO_2 micropowders (1.5 μm) were processed via EAM using a polymer–wax binder system (e.g., LDPE, EVA, paraffin wax, stearic acid)	Printed parts underwent two-stage de-binding, including solvent de-binding in heptane at 40 °C and thermal de-binding at 500 °C, followed by sintering at 900 °C for 3 h to obtain dense TiO_2 structures	51
	PbTe	Binder-free colloidal PbTe inks composed of Na-doped (p-type) or Sb-doped (*n*-type) PbTe particles were extrusion-printed without organic rheological additives	Printed objects were dried and subsequently heat-treated at 1,073 K under N_2 atmosphere to consolidate the thermoelectric material	52
L-DED	Si	Metallurgical-grade Si powder (98% purity) was processed by L-DED using a 600 W pulsed laser (1 ms pulse duration, 50 Hz) and a *z*-stage build speed of 0.1 mm s^{-1}. Deposition was performed on a heated plate set to 25–980 °C	NA	53

Abbreviations: 3D: Three-dimensional; AJP: Aerosol jet printing; Ar: Argon; EAM: Extrusion-based additive manufacturing; EHD-RP: Electrohydrodynamic redox printing; EVA: Ethylene-vinyl acetate; Ga: Gallium; GaN: Gallium nitride; GRAM: Gas-phase reactive additive manufacturing; IJP: Inkjet printing; LDPE: Low-density polyethylene; L-DED: Laser directed energy deposition; NA: Not available; PbTe: Lead telluride; Si: Silicon; SiO_2: Silicon dioxide; Ti: Titanium; TiO_2: Titanium dioxide; TPL: Two-photon lithography; Zn: Zinc; ZnO: Zinc oxide; Au: Gold.

2. Additive manufacturing for fabricating semiconductors

To date, only a limited set of semiconductor materials has been successfully fabricated using AM, and these materials and their associated AM techniques are systematically summarized in Table 1 and shown in Figure 2, respectively. In the following subsections, each AM process is briefly introduced, along with its main advantages and inherent limitations when applied to semiconductor materials.

Although the present discussion has focused on AM routes, it is important to recognize that semiconductor processing shares conceptual overlap with the ceramic community, where powder-based consolidation techniques—such as pressureless sintering, hot pressing, and spark plasma sintering—have long been employed. Many oxide semiconductors are mechanically and thermally closer to ceramics than to ductile metals, and therefore their response to rapid thermal cycles during AM may resemble ceramic processing behavior. In this context, insights from conventional ceramic densification, such as diffusion-controlled neck growth, grain-boundary mobility, pore elimination kinetics, and thermal shock resistance, may provide a valuable framework for interpreting densification and cracking phenomena in semiconductor AM. Establishing clearer connections between ceramic processing science and AM could therefore accelerate the development of more robust processing strategies for brittle semiconductor systems in the future.

2.1. Laser powder bed fusion

Laser PBF (L-PBF), often referred to as selective laser melting, is an AM technique in which 3D components are fabricated through the successive consolidation of powder layers using a focused laser heat source[31] (Figure 2A). The process begins with the creation of a digital 3D model, which is computationally discretized into a series of 2D cross-sectional layers. During fabrication, a thin layer of powder is uniformly spread across a build platform, after which a scanning laser selectively irradiates predefined regions to locally melt or fuse the powder according to the corresponding digital slice. Once a layer is completed, the build platform is incrementally lowered, and a fresh powder layer is deposited. The laser scanning and fusion sequence is then repeated, enabling metallurgical bonding between adjacent layers and the gradual vertical buildup of the component.[28] Through this iterative layer-wise approach, L-PBF enables the production of geometrically complex structures with high spatial resolution.[58-62]

Selective laser sintering (SLS) follows the same fundamental layer-wise manufacturing principle as L-PBF, involving the sequential deposition of powder layers and selective laser scanning based on sliced digital data. The key distinction lies in the laser–matter interaction mechanism. SLS typically employs lasers with longer wavelengths and lower energy densities, such that the powder particles are not fully melted; instead, partial melting or surface softening occurs, leading to bonding via solid-state diffusion or viscous flow at particle interfaces.[63] As a result, consolidation in SLS is achieved primarily via sintering mechanisms rather than complete melting, which reduces thermal gradients and residual stresses but generally yields parts with lower density and resolution compared to L-PBF.[64]

Laser PBF has been predominantly explored for the fabrication of TE semiconductor materials (Table 1), which enable direct conversion of heat into electrical energy at elevated temperatures.[65] A typical TE module consists of interconnected *n*-type and *p*-type semiconductor legs.[66] Conventional manufacturing of such modules relies on powder mixing and alloying via high-energy ball milling, followed by consolidation through hot pressing or spark plasma sintering and subsequent dicing into the desired geometries.[66] Notably, it has been reported that the dicing step alone can account for up to 50% material loss, arising from chipping, cracking, and kerf losses.[67,68] In addition, dicing inherently restricts achievable geometries to simple planar shapes (e.g., rectangular or square legs), limiting design freedom. This geometric constraint is particularly problematic because practical heat sources and sinks are often curved, resulting in suboptimal thermal contact and reduced device efficiency.[41] These limitations have motivated increasing interest in L-PBF as a route to reduce material waste while enabling complex, conformal, and non-planar thermoelectric architectures.

Despite these potential advantages, L-PBF processing of TE semiconductors remains extremely challenging, primarily due to their intrinsic material characteristics. The first major challenge is the lack of suitable powder feedstock. Many TE materials are not commercially available as spherical powders, which are generally required for stable powder spreading in L-PBF. For example, several studies reported unsuccessful or manual layer deposition owing to the irregular morphology and agglomeration of non-spherical powders (Figure 3A).[37,66,69-71] These powders are usually manufactured through ball milling and sieving of the ingot of the semiconductor material. Although some reports demonstrated that irregular powders could be deposited, the resulting parts typically exhibited low densification, in part due to the use of low laser powers and insufficient volumetric energy densities imposed by equipment limitations. For example, a maximum relative

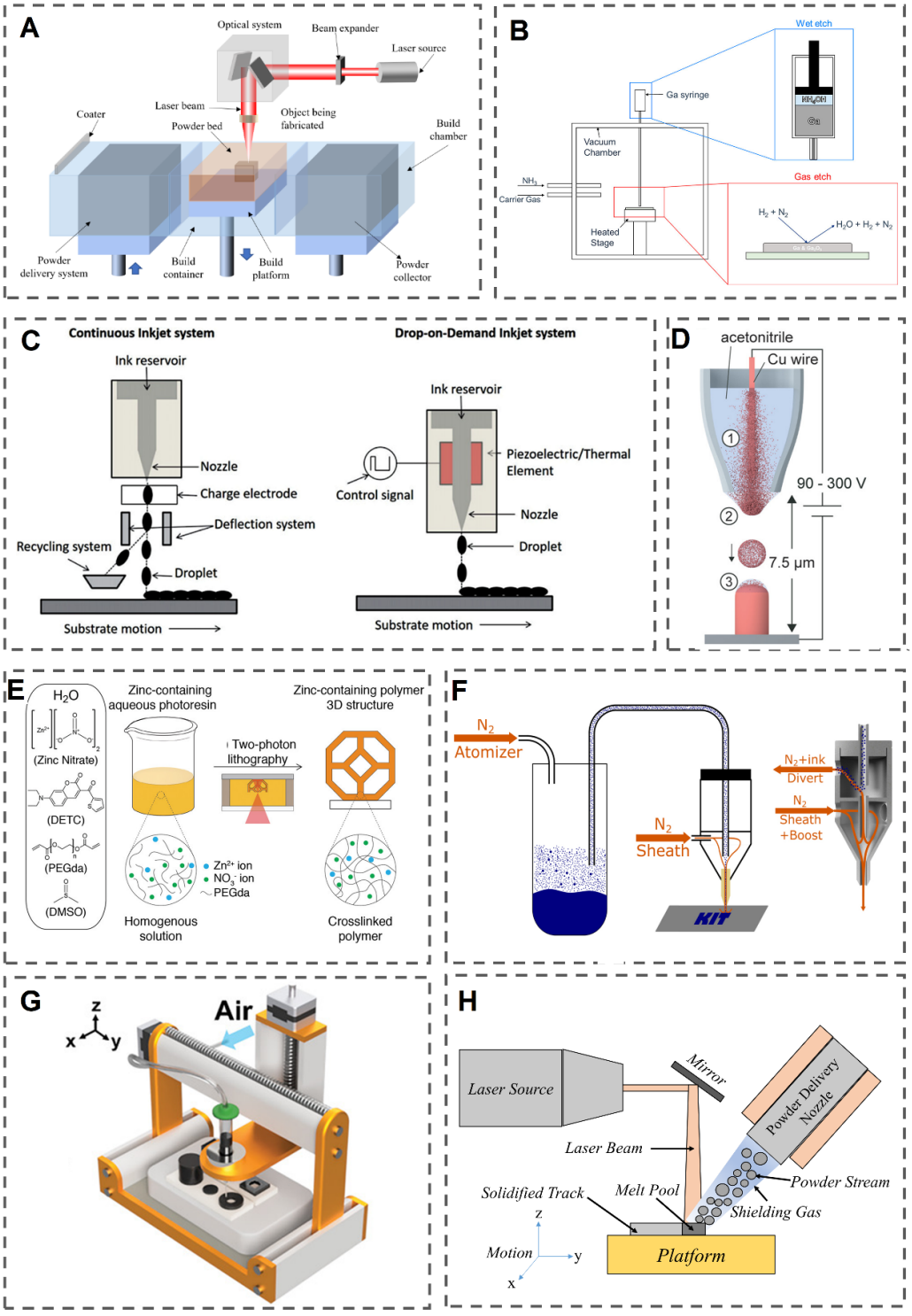

Figure 2. Schematic overview of additive manufacturing processes applied to semiconductor fabrication: (A) Laser power bed fusion (reproduced from Ref. 54), (B) gas-phase reactive additive manufacturing (reproduced with permission from Ref. 47, Copyright © 2024, American Chemical Society), (C) inkjet printing (reproduced from Ref. 55), (D) electrohydrodynamic redox printing (adapted from Ref. 56), (E) two-photon lithography (adapted from Ref. 23 with permission, Copyright © 2019, Wiley-VCH GmbH), (F) aerosol jet printing (adapted from Ref. 57), (G) extrusion-based additive manufacturing (reproduced from Ref. 52 with permission, Copyright © 2021, Wiley-VCH GmbH), and (H) laser directed energy deposition (created by the authors). Abbreviations: 3D: Three-dimensional; DETC: Diethyl thiophosphoryl chloride; DMSO: Dimethyl sulfoxide; PEGda: Poly(ethylene glycol) diacrylate.

density of only 77% (Figure 3B) has been reported for L-PBF-processed $Bi_2Se_{0.3}Te_{2.7}$[37] with cracks and porosities.

To address powder spreading issues, alternative strategies have been proposed, including gas atomization and the use of elemental powder blends dispersed in alcohol to form slurries, which can be uniformly deposited using a scraper. For the latter case, after deposition, the substrate is heated to evaporate the solvent prior to laser scanning.[38-40] Under appropriate processing conditions, self-propagating high-temperature synthesis, also referred to as in situ alloying, can occur during L-PBF, leading to the formation of the target TE compound.[39] While effective in improving layer uniformity, this approach introduces additional manual steps, increases processing time and cost, and may raise concerns regarding contamination and defect formation. In contrast, in situ alloying using dry elemental powder mixtures has also been demonstrated, notably for Sb_2Te_3[24], yielding homogeneous microstructures. Although this dry approach is more promising, suppressing compositional heterogeneity during in situ alloying remains a critical challenge, particularly given the stringent compositional control required for semiconductor performance.[37]

A second major challenge in L-PBF of TE semiconductor materials is crack formation induced by high thermal gradients and tensile residual stresses. Severe cracking has been reported in L-PBF-processed *n*-type $Si_{80}Ge_{20}$[41] and $Bi_2Se_{0.3}Te_{2.7}$ to a lesser extent (Figure 3B). However, the fundamental origins of cracking in TE materials have not yet been systematically investigated, highlighting the need for focused mechanistic studies in future work. In metallic L-PBF, cracking is commonly associated with mechanisms such as solidification cracking and liquation cracking at high temperatures, as well as solid-state phenomena, including strain-age cracking or cold cracking, particularly in martensitic steels.[31,72,73]

Cold cracking in such alloys is often linked to martensitic transformation-induced volumetric expansion and residual tensile stresses.[26] In contrast, many semiconductors and TE compounds are intrinsically brittle due to their predominantly covalent or partially ionic bonding, low fracture toughness, and limited dislocation mobility. As a result, classical hot or cold cracking phenomena established in metallic AM may not directly translate to semiconductor systems. Instead, cracking during semiconductor AM is expected to be dominated by thermal shock-induced fracture under steep thermal gradients, residual-stress–driven fracture in the absence of significant plastic strain accommodation (Figure 3B). This fundamental difference in deformation behavior suggests that defect mitigation strategies developed for metallic AM cannot be directly transferred to semiconductor AM without modification.

The third challenge concerns microstructural anisotropy and compositional heterogeneity in L-PBF–fabricated components. L-PBF of $Bi_2Se_{0.3}Te_{2.7}$, for example, resulted in highly textured columnar grains (Figure 3C).[37] The pronounced texture introduced strong anisotropy in thermoelectric properties, while nanoscale inclusions and elemental redistribution (Figure 3D) altered carrier transport behavior. In particular, tellurium-rich regions were observed along grain boundaries, and the combined effects of sparse inclusions and elemental segregation led to a transition from *n*-type to *p*-type conduction, indicating a shift in the dominant charge carriers from electrons to holes. In addition, short-range ordering, widely reported in complex ceramics and high-entropy systems, can influence local bonding environments and defect energetics in additively manufactured semiconductors. Although short-range ordering has not yet been systematically examined in semiconductor AM, its potential impact on carrier transport and phase stability merits future investigation.[74,75]

A fourth limitation arises from selective vaporization of volatile elements, especially under high volumetric energy densities. For Bi_2Te_3-based systems, it has been reported that a single-phase compound can be obtained at a relatively low energy density of approximately 20 J/mm^3.[40] However, increasing the energy density to 40 J/mm^3 results in the formation of secondary phases such as Bi_4Te_5, while further increases to 66.7 and 80 J/mm^3 lead to substantial vaporization of tellurium and selenium, reducing the stoichiometric ratio and promoting the formation of BiTe.[40] These observations highlight that excessive heat input causes compositional deviations, phase segregation, and degradation of thermoelectric performance. Consequently, the lowest laser energy density compatible with acceptable part quality should be employed to minimize volatilization of anion species.

The fifth challenge concerns the thermal conductivity of semiconductors. Thermal conductivity is a key material parameter governing melt-pool dynamics, temperature gradients, and overall printing quality in semiconductor L-PBF. Compared with most structural metals, many semiconductors, particularly TE compounds, exhibit relatively low intrinsic solid-state thermal conductivity. This limited heat dissipation leads to higher peak temperatures, steeper thermal gradients, and longer melt-pool lifetimes during laser processing. The resulting thermal stresses can exceed the fracture strength of brittle semiconductor materials, promoting microcracking and residual-stress–driven fracture. For example, in Bi_2Te_3-based systems processed by L-PBF, the inherently low and strongly temperature-dependent thermal conductivity of the solid

phase has been associated with pronounced temperature gradients and crack formation. It has been suggested that substrate preheating may reduce these gradients by increasing the temperature of previously solidified layers, thereby moderating thermal shock during subsequent laser passes.[76] More broadly, the temperature dependence of thermal conductivity in many semiconductors introduces an additional degree of freedom not typically dominant in metallic AM. Control of substrate temperature, laser pulse characteristics (e.g., repetition rate and pulse width), and heat-input modulation may enable the reduction of transient stress accumulation. Systematic management of heat flow and thermal boundary conditions is therefore critical for improving densification and mitigating cracking in semiconductor AM.

Finally, for Si-based systems, L-PBF inherently produces polycrystalline microstructures[44], whereas most semiconductor applications require single-crystal Si to ensure optimal electronic performance. This fundamental incompatibility further constrains the applicability of L-PBF for conventional semiconductor device fabrication.

2.2. Gas-phase reactive additive manufacturing

Gas-phase reactive AM (GRAM) is an emerging AM approach for the 3D fabrication of compound semiconductors that combines localized deposition of a liquid precursor with layer-wise gas–solid chemical reactions (Figure 2B).[47] Conceptually, GRAM is rooted in the principles of liquid-phase epitaxy[77], in which a molten elemental precursor serves as the source material for crystal growth while a reactive gas supplies the complementary element required for compound formation.

In the GRAM process, a liquid precursor (e.g., molten metals such as gallium or other low-melting constituents) is first deposited in a spatially controlled manner to define an individual layer on a substrate. Each deposited layer is subsequently exposed to a reactive gas atmosphere (e.g., ammonia or other nitrogen-containing gases) at elevated temperature, enabling localized chemical conversion before deposition of the next layer. Through this repeated sequence of deposition and reaction, 3D structures are progressively built.[46] This approach allows geometric definition to be governed by the printing step, while phase formation and crystallization are dictated by reaction kinetics rather than bulk melting. By avoiding the direct melting of compound semiconductor feedstocks and decoupling material placement from gas-phase transport, GRAM offers a flexible and potentially energy-efficient route for AM of semiconductors with complex geometries.

This approach is particularly well suited for applications requiring epitaxial thin films of high-melting-point semiconductors, such as GaN (Table 2). In such cases, reaction-based fabrication routes are favored over the direct use of GaN feedstock for several fundamental reasons. First, powder-based processing, analogous to L-PBF, inevitably yields polycrystalline microstructures, which are incompatible with the stringent crystallographic requirements of most compound semiconductor devices. Second, heating GaN powder to near-melting temperatures leads to nitrogen loss, stoichiometric imbalance, and defect formation, driven by the large disparity in vapor pressures between gallium and nitrogen. In addition, the melting point of GaN is exceptionally high (approximately 2,500 °C), whereas commercial reactive synthesis routes enable GaN formation at substantially lower temperatures (<1,200 °C), offering significant reductions in energy consumption and processing costs.[46]

Despite these advantages, the technique faces several notable limitations. These include limited spatial resolution and dimensional fidelity due to droplet spreading, volumetric changes during gas–liquid reactions, and the formation of native oxide layers (e.g., Ga_2O_3). Moreover, the process often results in pronounced surface roughness, while regions outside the printed features may become polycrystalline, likely due to wetting effects or contamination. Finally, the relatively low production rate restricts scalability, making this method more suitable for thin-film or 2.5D structures rather than fully 3D architectures.[47]

2.3. Inkjet printing

Inkjet printing (IJP) is a digitally controlled material deposition technique in which discrete liquid droplets are generated and selectively delivered to a target substrate (Figure 2C). Depending on the mechanism used to form and control droplets, IJP is generally divided into two main approaches: continuous IJP and drop-on-demand IJP. In continuous inkjet systems, droplets are produced continuously from a nozzle, and electric fields are used to steer individual droplets either toward the substrate or away from the printing region for recirculation. While this method enables high-throughput deposition, it is inherently less efficient in terms of material usage. Drop-on-demand IJP, by contrast, generates droplets only at prescribed locations, making it a more material-efficient approach. In this mode, droplet ejection is typically achieved through rapid thermal actuation or by mechanical displacement using a piezoelectric element.[78-81] Owing to its mask-less operation, precise spatial control, and compatibility with a wide range of functional inks, IJP has been widely explored in semiconductor-related applications, particularly for 2D coating[82,83] and patterning, although its extension to true 3D fabrication remains limited.

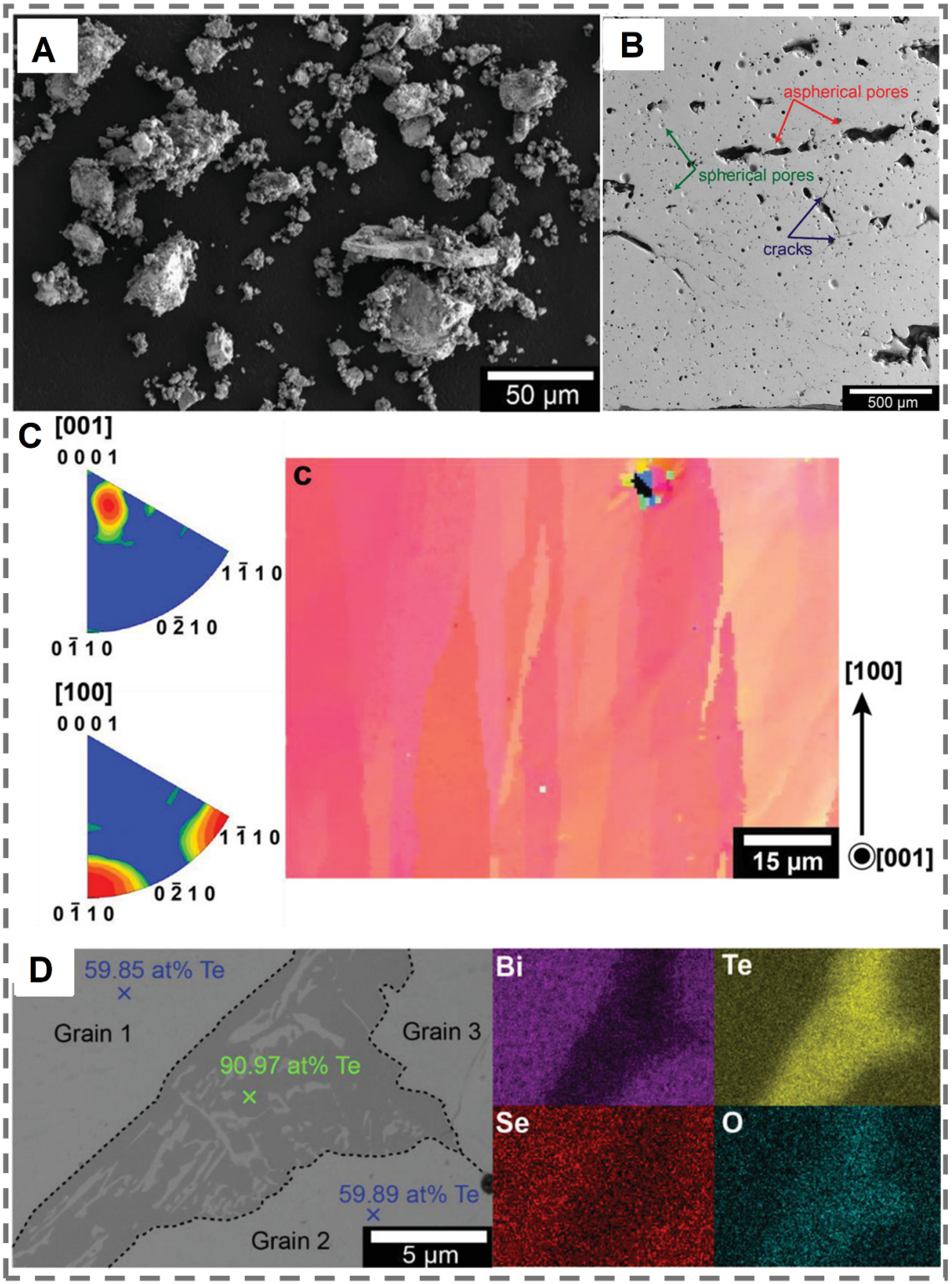

Figure 3. Microstructural challenges in laser powder bed fusion (L-PBF) of $Bi_2Se_{0.3}Te_{2.7}$ thermoelectric semiconductor: (A) irregular powder morphology (scale bar: 50 μm), (B) porosity and cracking in L-PBF fabricated part (scale bar: 500 μm), (C) strong texture (scale bar: 15 μm), and (D) elemental segregation (scale bar: 5 μm). Images adapted from Ref.[37]

Abbreviations: Bi: Bismuth; O: Oxygen; Se: Selenium; Te: Tellurium.

Although this technique has demonstrated encouraging performance for printing ZnO in sensor applications (Table 2), it is accompanied by several inherent limitations. First, the ink viscosity must be carefully controlled: excessively viscous inks can clog the nozzle, while low-viscosity formulations compromise dimensional accuracy; nozzle blockage is often associated with particle agglomeration within the orifice.[79] Second, residual precursor-related species, such as $Zn(OH)_2$, have been reported to persist after calcination, leading to shifts in the optical band gap of the resulting ZnO.[49] Third, the coffee-ring effect can induce non-uniform material distribution, producing uneven and inhomogeneous patterns that degrade printing resolution and spatial precision, particularly critical for miniaturized devices.[78] Fourth, internal stresses generated during post-print heat treatments may cause pattern distortion and surface wrinkling in the deposited films.[79] Finally, the presence of structural defects in the printed ZnO can further alter the electronic structure and adversely impact band-gap–related properties.

2.4. Electrohydrodynamic redox printing

Electrohydrodynamic redox printing (EHD-RP) is an electrochemical, high-resolution AM technique that enables the direct writing of dense metallic micro- and nanostructures through localized redox reactions (Figure 2D). In EHD-RP, metal ions are generated in situ by anodic dissolution of a sacrificial metal source within a liquid medium and are transported toward a conductive substrate by a strong electric field. Upon reaching the substrate, these ions are electrochemically reduced, forming a metallic deposit with sub-micron feature sizes.[84] Unlike many powder- or ink-based approaches, EHD-RP produces metallic structures directly during printing and therefore does not require post-deposition sintering or consolidation.[50] While the process inherently yields metals, semiconductor structures can subsequently be realized by controlled post-printing oxidation of the printed metallic features, converting them into their corresponding metal oxides.[50,85] Through this two-step route, namely electrochemical metal deposition followed by oxidation, EHD-RP provides an indirect yet highly precise pathway for fabricating semiconductor materials, particularly metal-oxide semiconductors.

This technique has been primarily applied to the fabrication of semiconducting materials for gas-sensing applications. EHD-RP offers a high printing throughput, reaching approximately 10 voxels/s with minimum voxel sizes of approximately 170 nm, outperforming other electrochemical printing approaches that typically achieve 1–3 voxels/s with comparable feature sizes.[86] A distinctive advantage of EHD-RP is its ability to dynamically control material chemistry during printing, enabling multi-metal deposition with chemical feature sizes below 400 nm. This capability arises uniquely from the in situ generation of metal ions from sacrificial anodes, which allows seamless switching between different metallic species within a single print.

The combination of high deposition speed and multi-material capability makes EHD-RP a promising platform for direct microscale fabrication. Moreover, the use of aqueous solvents provides substantial flexibility, as a wide range of metals can be dissolved and electrochemically redeposited. To date, copper and zinc have been successfully printed, which could subsequently be converted into their corresponding oxides through post-printing oxidation, yielding functional semiconductors. In principle, the compatibility of EHD-RP with aqueous systems could be extended to a broader range of metals. Furthermore, replacing sacrificial anodes with metal salt precursors may enable access to more noble metals that do not readily undergo corrosion in aqueous environments.[50]

Despite these advantages, several limitations currently restrict broader adoption. First, complete conversion of printed metals to oxides often requires prolonged oxidation times and elevated temperatures, and only partial oxidation has been done successfully to date. Second, thermal mismatch between the printed material and Si substrates during post-processing can lead to deformation, distortion, or fracture, undermining shape fidelity and structural integrity. Collectively, these challenges constrain the practical applicability of EHD-RP for robust semiconductor manufacturing.[50]

2.5. Two photon lithography

Two-photon lithography (TPL) is a high-resolution AM technique capable of producing complex 3D micro- and nanostructures through localized two-photon-induced photopolymerization (Figure 2E). In TPL, a tightly focused laser induces polymerization only at the focal volume via a nonlinear optical process, enabling feature sizes well below 1 μm and true 3D freeform fabrication.[35] For semiconductor-related applications, TPL is commonly combined with specially designed photoresins that contain metal-bearing species or inorganic building blocks. During printing, these photoresins are patterned into 3D polymer architectures that spatially define the desired geometry. Subsequent thermal treatment converts the printed structures into their corresponding inorganic or metal-oxide forms by removing the organic matrix and inducing oxide formation.[23] This indirect fabrication route allows TPL to overcome limitations associated with light scattering from solid particles and enables the creation of

monolithic semiconductor microstructures with arbitrary geometry and exceptionally high resolution. As a result, TPL-based AM has emerged as a powerful approach for fabricating 3D semiconductor and metal-oxide architectures that are difficult or impossible to realize using conventional lithographic or deposition techniques.

This technique demonstrates strong potential for fabricating 3D micro- and nanoscale structures, as evidenced by reports of nano-architected ZnO geometries with feature sizes down to approximately 250 nm (Figure 4). The presented slurry-free, photolithography-based approach for producing monolithic 3D ZnO architectures represents a substantial simplification compared with existing methods, while enabling structural designs and device concepts that were previously unattainable. An additional advantage of this process lies in its ability to control linear shrinkage during calcination through selective leaching of zinc ions, providing an effective secondary route for enhancing structural resolution, enabling size reductions of up to 70–90%. This capability marks a notable advancement beyond the current state of the art and opens a pathway toward the realization of previously inaccessible 3D piezoelectric microstructures.[23]

Despite these promising results, the applicability of this technique remains constrained. To date, its use has been largely limited to ZnO, with little information available on its extension to other semiconductor materials (Table 2). In addition, the process involves multiple fabrication and post-processing steps, and potential contamination introduced during processing may adversely affect semiconductor performance. Moreover, commonly used photoresists are liquid organic polymer systems with critical feature sizes typically limited to around 80–100 nm and with limited resistance to aggressive pattern-transfer conditions, making them unsuitable for many chip- and device-level applications.[87]

2.6. Aerosol jet printing

Aerosol jet printing (AJP) is a direct-write deposition technique that fabricates patterns by delivering an aerosolized stream of liquid ink onto a substrate with high spatial control (Figure 2F). In this approach, a liquid ink is first converted into fine droplets through an atomization process, forming an aerosol that is transported by a carrier gas toward the deposition nozzle. A secondary gas flow, commonly referred to as a sheath gas, surrounds and focuses the aerosol stream, effectively acting as a virtual nozzle that confines the material jet before it reaches the substrate. This gas-assisted focusing enables precise feature definition and reduces the likelihood of nozzle clogging compared with conventional IJP.[88-90] One of the key advantages of AJP is its broad ink compatibility, as it can accommodate a wide range of ink viscosities and material systems, including polymers, metals, and semiconductor-related inks. Owing to its mask-less operation, fine feature resolution, and flexibility in ink formulation, AJP has been widely explored for electronic and semiconductor applications, particularly for 2D patterning.[91] While aerosol jet/aerosol-gel printing is predominantly used for 2D and conformal 2.5D patterning, multiple studies have demonstrated true 3D, *Z*-directional buildup at the micro-scale (e.g., freestanding pillars, walls, and lattice-like microarchitectures) through layer-by-layer stacking and/or rapid curing/solidification mechanisms.[20]

Recent studies have demonstrated that the technique can be extended to produce complex 3D ZnO microlattice architectures and micropillars with intricate geometries (Figure 5A), suitable for applications such as cancer biomarker sensing. In addition, this process has shown promising potential for multimaterial 3D fabrication, including ZnO–TiO_2 systems (Figure 5B) and hybrid Al_2O_3–TiO_2–ZnO ceramic structures (Figure 5C), thereby highlighting its versatility for functional microarchitected materials.[20]

2.7. Extrusion-based additive manufacturing

Extrusion-based AM (EAM) is a material deposition technique in which a viscoelastic feedstock, typically formulated as a paste, slurry, or ink, is dispensed through a nozzle and deposited in a programmed, layer-by-layer manner to build 3D structures (Figure 5G). In this approach, functional powders are first dispersed within a liquid or polymeric binder to produce an extrudable ink with suitable rheological properties for continuous flow and shape retention after deposition. During printing, the ink is delivered from a reservoir or syringe through nozzles of defined diameter using pressure- or mechanically driven extrusion, while the motion of the print head or substrate defines the desired geometry. Following deposition, printed structures generally undergo drying to remove solvents and subsequent thermal treatment to eliminate organic constituents, promote particle bonding, and develop the final functional material properties. Owing to its simplicity, material versatility, and compatibility with highly loaded functional inks, EAM has been widely explored for the fabrication of ceramic, metallic, and semiconductor-related components, particularly where complex geometries and compositional flexibility are required.[51,52,92-94]

Using this approach, TiO_2 semiconductors for photocatalytic CO_2 reduction, as well as PbTe thermoelectric materials, have been successfully fabricated

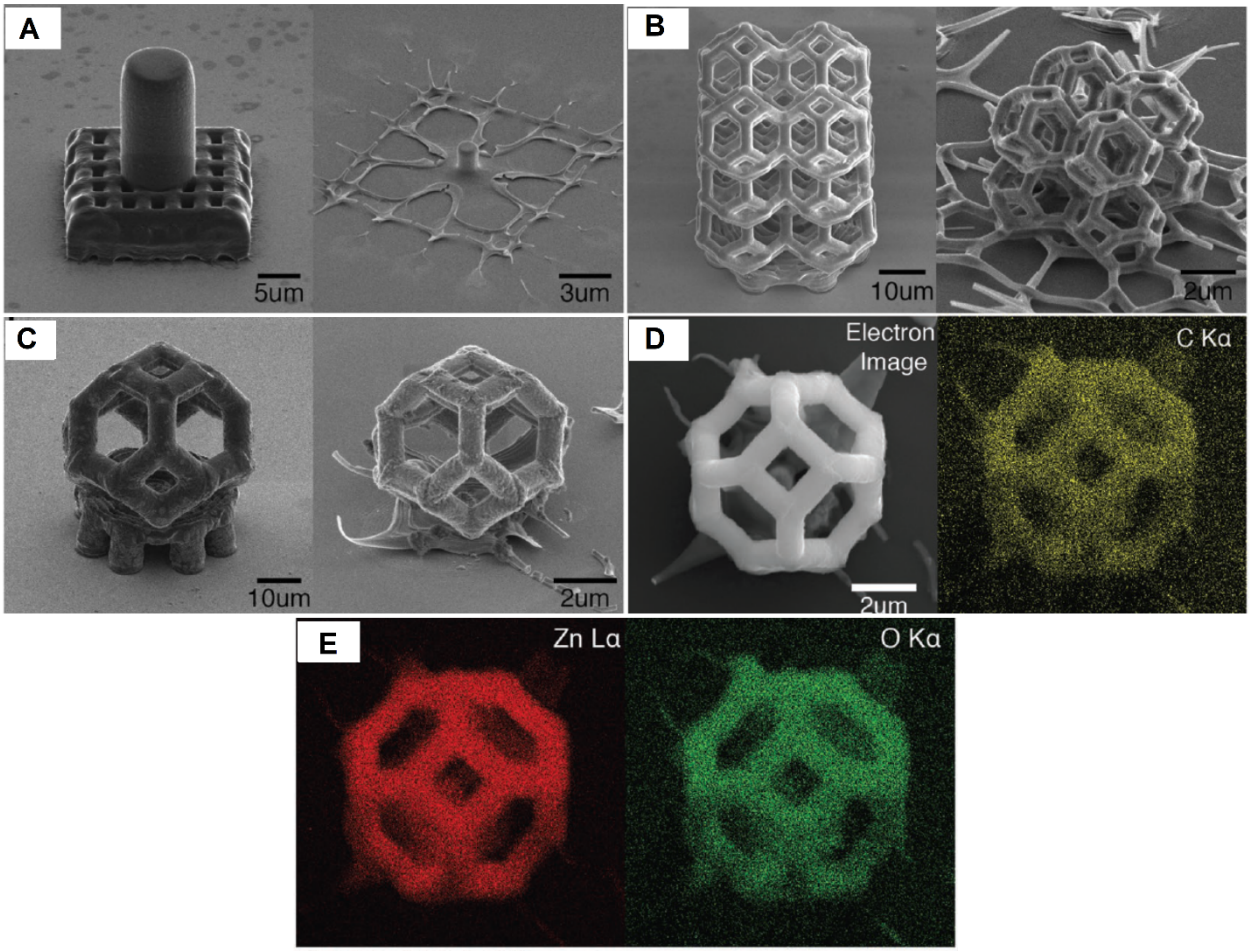

Figure 4. Representative scanning electron microscopy images showing: (A) a single cylindrical pillar (left: scale bar = 5 μm; right: scale bar = 3 μm), (B) a microlattice composed of tetrakaidecahedral units (left: scale bar = 10 μm; right: scale bar = 2 μm), and (C) an individual tetrakaidecahedron fabricated by two-photon lithography using an aqueous zinc ion photoresin (left: scale bar = 10 μm; right: scale bar = 2 μm), shown before (left) and after (right) calcination. All structures exhibit a uniform linear shrinkage of 87 ± 2% following calcination. (D, E) Energy-dispersive X-ray spectroscopy elemental maps of zinc (Zn), carbon (C), and oxygen (O) for a calcined tetrakaidecahedron unit cell. Images adapted from Ref.[23] with permission, Copyright © 2019, Wiley-VCH GmbH.

(Table 2).[51,52] Despite these encouraging demonstrations, the broader applicability of EAM to semiconductors remains limited. Inks or feedstocks suitable for many semiconductor materials are not readily available, and the process typically requires multiple post-processing steps (e.g., debinding and sintering), which can compromise dimensional fidelity and structural integrity. Furthermore, the achievable resolution and minimum feature size are generally on the order of hundreds of micrometers, rendering this technique unsuitable for applications demanding fine features, such as microelectromechanical systems and nanoelectronic devices.

2.8. Laser directed energy deposition

Laser-directed energy deposition (L-DED) is an AM process in which a concentrated energy source, most commonly a laser, is used in conjunction with a controlled material delivery system to fabricate 3D components (Figure 2H). In this technique, feedstock material, supplied in the form of powder or wire, is delivered directly into the laser–material interaction zone, where it is rapidly heated and melted.[31,95] The molten material is deposited onto a substrate or previously solidified layer, where it solidifies and forms a metallurgical bond. By moving the deposition head or substrate along predefined toolpaths, material is laid

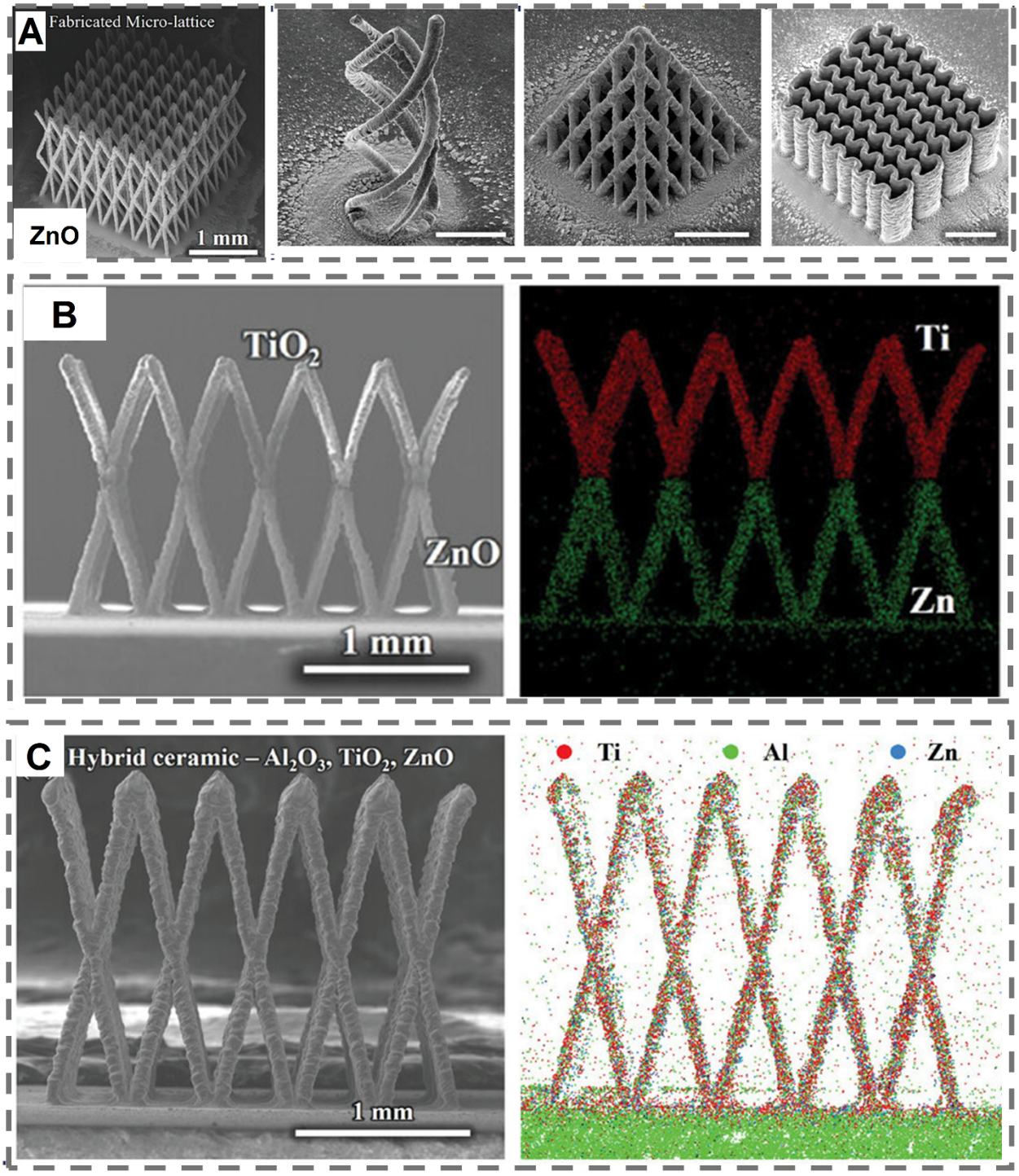

Figure 5. Monomaterial and multimaterial ceramic microarchitectures fabricated by aerosol jet printing demonstrating complex three-dimensional structures and spatially resolved compositional control. (A) Representative three-dimensional microarchitectures fabricated by aerosol jet printing, including ZnO microlattices (scale bar: 1 mm), multispiral structures (scale bar: 500 μm), pyramidal microlattices (scale bar: 500 μm), and wavy microwalls with nanoscale features (scale bar: 500 μm). (B) A bimaterial microlattice consisting of a TiO_2 upper region and a ZnO lower region, with EDX analysis confirming spatially resolved composition. (C) Hybrid ceramic microlattices composed of Al_2O_3, TiO_2, and ZnO, with EDX maps demonstrating a homogeneous distribution of Ti, Al, and Zn throughout the structure. Images adapted from Ref.[20]
Abbreviations: Al: Aluminum; Al_2O_3: Aluminum oxide; EDX: Energy-dispersive X-ray; Ti: Titanium; TiO_2:Titanium dioxide; Zn: Zinc; ZnO: Zinc oxide.

down in a track-by-track and layer-by-layer manner until the desired geometry is achieved.[96] Owing to its ability to deposit material precisely and dynamically, L-DED is well-suited for large-scale component fabrication, component repair, and the additive buildup of relatively complex 3D structures.

The application of L-DED to semiconductor fabrication remains extremely limited. To date, only a single study has reported the 3D printing of pillars from metallurgical-grade Si powder (98% purity) deposited onto Si substrates (Table 2).[53] This limited adoption is not unexpected, as L-DED is inherently optimized for high deposition rates and large-scale components, rather than the fine feature resolution and tight dimensional tolerances required in semiconductor manufacturing.[31] Consequently, L-DED is better suited for producing tooling, fixtures, or equipment components used in conventional semiconductor processing, rather than functional semiconductor devices themselves.

When applied to semiconductors, L-DED faces several fundamental challenges. These include insufficient dimensional accuracy, formation of inclusions during deposition, and crack formation driven by high thermal gradients in combination with the brittle nature of most semiconductor materials. Even for Si, severe interfacial cracking has been reported despite the use of substrate preheating up to 980 °C, underscoring the intrinsic difficulty of processing brittle semiconductors using this high-energy, melt-based technique.[53]

3. Future roadmap

3.1. Outlook for cm–mm-scale semiconductor fabrication by laser powder bed fusion

Collectively, it is evident that the AM of semiconductors is still at a nascent stage. To date, only a limited number of studies have been reported, many of which have struggled to produce defect-free, application-ready semiconductor components that can compete with their conventionally manufactured counterparts. Nevertheless, the progress achieved so far, particularly for thermoelectric materials, demonstrates significant promise. Building on the identified challenges, a roadmap for future research is outlined below.

For cm–mm-scale semiconductor components with sub-mm features, particularly in the context of thermoelectric materials, L-PBF remains the most promising AM technique. However, fully realizing its potential requires coordinated advances across materials, processing, and post-processing. Key research directions include:

(a) Development of compatible substrates

Laser PBF relies on depositing and melting powder layers onto compatible or compositionally matched substrates to ensure metallurgical bonding and to mitigate cracking. For many thermoelectric semiconductors, such substrates are currently unavailable. Future work should focus on producing composition-matched substrates via conventional routes such as liquid metallurgy, hot pressing, or spark plasma sintering.

(b) Production of L-PBF-grade semiconductor powders

High-quality powder feedstock is critical. Gas-atomized, spherical semiconductor powders with well-controlled particle size distributions must be developed. These powders should be systematically characterized in terms of flowability, packing density, laser absorptivity, oxygen content, and spreading behavior, parameters that remain largely unexplored for most semiconductor systems.

(c) Comprehensive process–structure–property–performance relationships

A systematic investigation of L-PBF process parameters across a wide range of semiconductors is required to optimize density, stoichiometric stability, control elemental evaporation, impurity levels, inclusions, surface quality, microstructural homogeneity, and crystallographic texture. These microstructural features must then be quantitatively correlated with electrical, thermal, mechanical, and thermoelectric performance.

(d) Post-build heat treatment and surface engineering

Tailored post-processing strategies, including heat treatments, annealing under controlled atmospheres, and surface finishing, are needed to refine microstructure, reduce defects, and achieve application-specific surface quality. Unlike metallic AM, where stress-relief and tempering treatments are routinely used to mitigate cracking and microstructural defects, the role of post-processing in semiconductor AM remains largely unexplored. Future research should systematically investigate whether controlled annealing can reduce residual stresses without inducing volatile element loss, dopant redistribution, phase segregation, or degradation of electronic properties. Establishing semiconductor-specific heat-treatment protocols represents a critical step toward defect mitigation and device reliability.

(e) Laser-based surface doping and modification

The feasibility of post-build laser surface doping or laser-assisted compositional modification within L-PBF platforms should be explored as a route to locally tune carrier concentration and functional gradients in semiconductor components.

(f) Geometric complexity beyond bulk ingots

Future studies should move beyond simple bulk or ingot-like geometries and exploit L-PBF's design freedom to fabricate complex, architected, and conformal semiconductor structures with functional advantages, such as improved thermal contact or enhanced transport properties.

(g) In situ alloying using elemental powder blends

The use of elemental powder mixtures for in situ alloying during L-PBF offers a flexible pathway for compound semiconductor fabrication. However, strategies to suppress compositional heterogeneity and phase segregation must be developed to meet the stringent requirements of semiconductor performance.

(h) High-temperature build platforms to mitigate cracking

Printing under elevated build-plate temperatures should be systematically investigated to reduce thermal gradients, mitigate residual stresses, and suppress cold cracking in brittle semiconductor materials.

(i) Atmosphere engineering during L-PBF

The development of controlled build atmospheres beyond inert Ar or N_2, including the use of anion-rich or semi-reactive atmospheres (e.g., Te- or Se-containing vapor overpressure), to suppress selective evaporation, stabilize stoichiometry, and mitigate phase segregation during L-PBF of volatile compound semiconductors.

(j) Texture and crystallographic orientation engineering

A systematic exploration of scan strategies, energy input modulation, and thermal gradients to deliberately control crystallographic texture and grain orientation, enabling alignment of anisotropic electrical and thermal transport properties with device-relevant directions in thermoelectric components.

(k) Defect and vacancy engineering as a functional design variable

A transition from defect suppression toward intentional control of point defects, antisite defects, and vacancy concentrations via L-PBF processing parameters, with the goal of tuning carrier concentration, phonon scattering, and overall thermoelectric performance.

(l) Hybrid L-PBF–solid-state transformation routes

The adoption of processing strategies in which L-PBF is used to fabricate near-net-shape, metastable bulk geometries, followed by controlled post-build solid-state transformations (e.g., ordering, precipitation, phase separation) to achieve the desired semiconductor phase constitution and functional properties.

(m) Functionally graded semiconductor architectures

The exploitation of L-PBF's spatial control to fabricate compositionally or dopant-graded semiconductor components, including graded n–p regions, thermal-expansion-matched interfaces, or property gradients within individual thermoelectric legs.

(n) Reliability, thermal cycling, and long-term stability assessment

A systematic evaluation of thermal fatigue, dopant diffusion, microstructural stability, and performance degradation under realistic service conditions to establish the long-term viability of L-PBF-fabricated semiconductor components.

3.2. Outlook for sub-mm to micro-scale semiconductor fabrication

At the sub-mm to micro-scale, AM processes (e.g., GRAM, IJP, AJP, and EAM) offer promising pathways for fabricating functional semiconductor structures and devices. However, further progress requires targeted advances in the following areas:

(i) Improved dimensional fidelity and resolution control: For GRAM and ink-based techniques, future work should focus on mitigating droplet spreading, wetting effects, and volumetric changes during reactions or drying, through optimized rheology, surface energy engineering, and substrate functionalization.

(ii) Expansion of printable semiconductor material libraries: The development of stable, printable inks or precursors for a broader range of semiconductors beyond ZnO, TiO_2, and PbTe is critical. This includes compound semiconductors, doped systems, and functional heterostructures with controlled composition.

(iii) Advanced ink and precursor chemistry design: Future efforts should emphasize binder-free or low-residue formulations, controlled decomposition pathways, and precursor systems that minimize residual phases, impurity incorporation, and band gap perturbations after post-processing.

(iv) Reduction of post-processing complexity and damage: Multi-step thermal treatments (e.g., calcination, debinding, and oxidation) should be streamlined or partially integrated into the printing process to reduce internal stresses, cracking, and loss of structural integrity.

(v) Controlled microstructure and phase formation: Systematic studies linking printing parameters to grain size, porosity, phase purity, and defect

density are needed to establish process–structure–property relationships at the micro-scale.

(vi) True 3D device architectures beyond 2D/2.5D patterning: While many ink-based techniques are currently used for planar or quasi-3D structures, future work should emphasize freestanding microstructures, vertical integration, and multilayer stacking, enabling functional 3D semiconductor devices.

(vii) Multimaterial and heterostructure integration: Building on early demonstrations (e.g., ZnO–TiO_2, hybrid oxide systems), research should explore spatially resolved multimaterial printing for junction formation, sensing platforms, and integrated device architectures.

(viii) Reliability and device-level validation: Beyond proof-of-concept structures, future studies must address long-term stability, thermal cycling, electrical reliability, and environmental robustness of sub-mm and micro-scale printed semiconductor devices.

3.3. Outlook for sub-micron to nanoscale semiconductor fabrication

For feature sizes below 1 μm, EHD-RP and TPL represent the most promising AM routes. At these length scales, the focus shifts from bulk fabrication to precision, functionality, and device-level integration.

(i) Broadening material diversity beyond metal oxides: To date, both EHD-RP and TPL have been demonstrated primarily for ZnO and a limited set of metal oxides. Future work should explore new semiconductor chemistries, including doped oxides, compound semiconductors, and mixed-anion systems.

(ii) Lower-temperature and faster post-conversion routes: For EHD-RP, strategies to achieve complete and uniform oxidation at reduced temperatures and shorter times are essential to prevent substrate damage and structural distortion. Similarly, TPL-derived structures would benefit from lower-temperature inorganic conversion routes.

(iii) Mitigation of thermal mismatch and substrate damage: At the nanoscale, thermal expansion mismatch between printed structures and substrates (e.g., Si) can cause distortion or fracture. Future work should explore buffer layers, compliant substrates, and low-stress conversion pathways.

(iv) Reduction of contamination and residue effects: In TPL, contamination arising from photoresist decomposition and residual organics remains a major concern. Development of inorganic-rich or hybrid photoresists with cleaner conversion chemistry is a critical research direction.

(v) Pushing resolution beyond current photoresist limits: Since conventional photoresists impose critical dimension limits (approximately 80–100 nm), future efforts should focus on novel resist chemistries, alternative photoinitiators, and shrinkage-engineering strategies to further enhance resolution.

(vi) Direct semiconductor printing without indirect conversion: A major long-term goal is to reduce reliance on indirect routes (metal → oxide or polymer → oxide) and enable the direct printing of functional semiconductors with controlled stoichiometry and electronic properties.

(vii) Integration with conventional micro/nanofabrication: Future research should emphasize hybrid fabrication workflows, combining EHD-RP or TPL with lithography, etching, and thin-film deposition to enable device-level integration rather than standalone structures.

4. Conclusion

Additive manufacturing of semiconductors remains in its infancy, yet the progress summarized in this perspective highlights its growing potential as a complementary fabrication paradigm, rather than a direct replacement for conventional semiconductor fabrication. By critically assessing current AM processes across relevant length scales, this perspective emphasizes that AM offers unique value, particularly in architected thermoelectric components, microstructured sensors, and nano-enabled functional devices, even as fundamental challenges persist. The proposed roadmap underscores that future success will rely on co-design of materials, processes, and device architectures, as well as tighter integration with established semiconductor manufacturing workflows. As these directions mature, AM is poised to expand the design space of semiconductor devices beyond planar constraints, enabling new functionalities that are inaccessible through traditional fabrication routes.

Acknowledgments

None.

Funding

None.

Conflict of interest

Swee Leong Sing is the Editor-in-Chief of this journal, but was not in any way involved in the editorial and peer-review process conducted for this paper, directly or indirectly. Separately, other authors declared that they have no known competing financial interests or personal relationships that could have influenced the work reported in this paper.

Author contributions

Conceptualization: All authors
Visualization: Ali Ghasemi
Writing – original draft: Ali Ghasemi
Writing – review & editing: All authors

Ethics approval and consent to participate

Not applicable.

Consent for publication

Not applicable.

Availability of data

Not applicable.

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