

ARTICLE

Noise coupling analysis of through-silicon via-based three-dimensional integrated circuits using carbon nanotube interconnects and Teflon dielectric for high-frequency applications

Prathap Reddy Pathakunta Guru^{1*}, and Sravan Abhilash Kothapalli²¹Department of Electronics and Communication Engineering, Bharatiya Engineering Science and Technology Innovation University, Sri Sathya Sai District, Andhra Pradesh, India²Department of Electronics and Communication Engineering, CMR Engineering College, Hyderabad, Telangana, India

Abstract

Conventional two-dimensional integrated circuits are increasingly limited by interconnect delays, power density, and scaling constraints predicted by Moore's law. Three-dimensional (3D) integrated circuits (ICs), enabled by through-silicon via (TSV) technology, overcome these limitations by vertically stacking dies, thereby reducing interconnect lengths, increasing bandwidth, enhancing functionality, and allowing higher integration density. However, noise coupling in TSV-based 3D ICs significantly impacts signal integrity, especially at high operating frequencies. This study proposes replacing the traditional dielectric silicon dioxide (SiO₂) with Teflon due to its lower dielectric constant and higher thermal resistivity. It provides a comprehensive comparative analysis of copper (Cu), carbon nanotube (CNT), and conventional semiconductor core materials using both single-liner and stacked-liner configurations with SiO₂ and Teflon dielectrics at 10 GHz and 1 THz. Noise coupling is assessed in terms of electric potential and expressed as attenuation in dB. Results show that CNT interconnects consistently display lower noise coupling than metallic and semiconductor cores. At 10 GHz and 4 μm arc length, Teflon–CNT achieves 10.75 dB compared to 5.03 dB for SiO₂–Cu. At 1 THz, attenuation decreases to 13.56 dB, representing an 8.53 dB reduction relative to Cu. Although SiO₂ remains an industry-standard dielectric, the Teflon-based stacked configuration offers superior high-frequency isolation. Consequently, the CNT–Teflon structure emerges as a promising solution for next-generation high-performance 3D IC systems beyond conventional scaling limits.

Keywords: Teflon; Carbon nanotube; Through-silicon via; Noise coupling; Electrical interference; Three-dimensional integrated circuit

***Corresponding author:**Prathap Reddy Pathakunta Guru
(2023sece007@bestiu.edu.in)

Citation: Guru, P. R. P. & Kothapalli, S. A. (2026). Noise coupling analysis of through-silicon via-based three-dimensional integrated circuits using carbon nanotube interconnects and Teflon dielectric for high-frequency applications. *Int J Systematic Innovation*, 10(3): 026130034. [https://doi.org/10.6977/IJoSI.202606_10\(3\).0006](https://doi.org/10.6977/IJoSI.202606_10(3).0006)

Received: March 25, 2026**Revised:** April 23, 2026**Accepted:** May 12, 2026**Published online:** June 26, 2026

Copyright: © 2026 Author(s). This is an Open-Access article distributed under the terms of the Creative Commons Attribution License, permitting distribution, and reproduction in any medium, provided the original work is properly cited.

Publisher's Note: AccScience Publishing remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

1. Introduction

Over the past several decades, the continuous scaling of semiconductor devices has been guided by Moore's law, which predicts that the number of transistors integrated on a chip approximately doubles every two years, leading to higher performance and

reduced cost per transistor (Wang *et al.*, 2019). However, as device dimensions approach the nanometer regime, conventional two-dimensional (2D) integrated circuits (ICs) are increasingly facing critical challenges, including interconnect delays, high power density, signal-integrity degradation, and thermal management issues. In modern ICs, interconnect delay has become a dominant factor limiting system performance, thereby restricting further scaling of planar architectures (Koester *et al.*, 2008). To overcome these limitations, three-dimensional (3D) ICs have emerged as a promising technology that enables vertical stacking of multiple semiconductor dies. In 3D IC architectures, stacked dies are interconnected using vertical interconnect structures known as through-silicon vias (TSVs) (Zheng *et al.*, 2016). Compared with traditional 2D ICs, 3D ICs provide several advantages, including reduced interconnect length, higher bandwidth, improved performance, lower power consumption, and increased integration density. Additionally, 3D integration enables heterogeneous integration of different functional components such as processors, memory modules, sensors, and radio frequency circuits within a compact footprint, making it highly suitable for applications such as high-performance computing, artificial intelligence hardware, and advanced communication systems (Cao *et al.*, 2021). A typical TSV-based 3D IC architecture is illustrated in Figure 1. In this structure, multiple semiconductor dies are vertically stacked and electrically connected using TSVs. Each die contains device layers and metal interconnect layers, while TSVs provide vertical electrical paths between stacked layers. The stacked dies are integrated onto a silicon interposer, enabling high-density signal routing and efficient communication between functional blocks. Beneath the interposer, the substrate and circuit

board provide mechanical support and external electrical connectivity (Rafi *et al.*, 2023). This architecture allows the integration of multiple dies, such as processors, memory units, and other functional modules, within a single compact package, thereby improving system performance and functionality.

Through-silicon vias play a crucial role in enabling vertical signal transmission between stacked dies in 3D ICs. TSVs significantly reduce interconnect lengths compared with conventional wire bonding and flip-chip techniques, thereby reducing propagation delay and improving signal bandwidth (Hu *et al.*, 2019). Moreover, TSV-based integration improves system-level performance and enables compact system-on-chip architectures. Despite these advantages, TSV technology also introduces several challenges, including thermal management issues, mechanical stress due to coefficient-of-thermal-expansion mismatch, electromigration, and noise coupling between adjacent TSVs (Xu *et al.*, 2025). Among these challenges, noise coupling is one of the most critical factors affecting signal integrity in TSV-based 3D ICs, particularly at high operating frequencies. When TSVs are placed in close proximity, capacitive and inductive coupling between neighboring TSVs can cause signal interference and degrade electrical performance. In addition, coupling between TSVs and the silicon substrate further contributes to signal distortion in high-speed circuits operating in the gigahertz and terahertz frequency ranges (Avouris *et al.*, 2007). Conventionally, silicon dioxide (SiO₂) has been widely used as the dielectric liner material surrounding TSV structures due to its good electrical insulation and compatibility with the complementary metal-oxide-semiconductor (CMOS) fabrication processes. However, the relatively high dielectric constant of SiO₂ ($k \approx 3.9$)

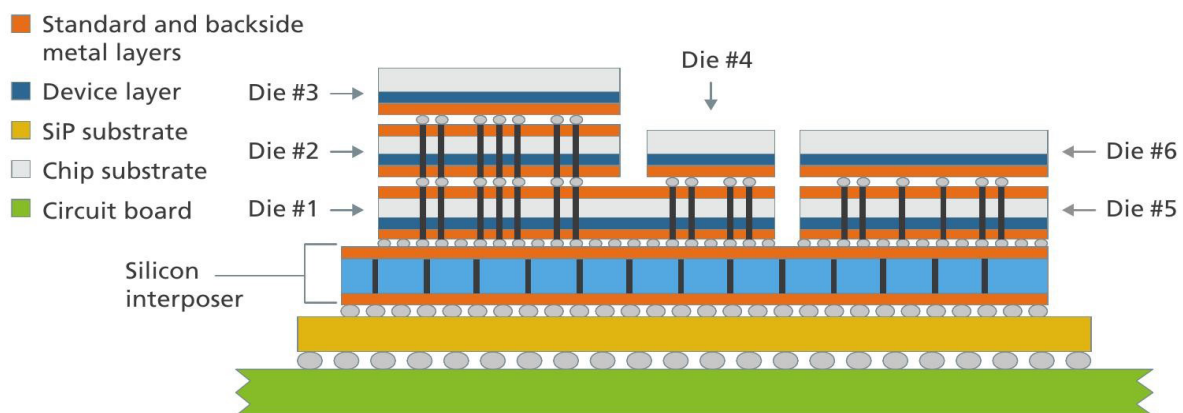


Figure 1. Architecture of a through-silicon via (TSV)-based three-dimensional integrated circuit showing vertically stacked dies interconnected through TSVs and integrated on a silicon interposer. Adapted from Cadence PCB Solutions (2018).

increases capacitive coupling between adjacent TSVs, leading to greater noise interference in high-frequency applications (Yasmin *et al.*, 2022). Therefore, alternative low-dielectric-constant materials are being explored to improve electrical isolation and reduce coupling effects in TSV structures. One such promising material is Teflon (Teflon AF 1600), which exhibits an ultra-low dielectric constant and high thermal resistivity (Chandrakar & Majumder, 2022). These properties make Teflon highly suitable for reducing capacitive coupling and improving signal integrity in high-frequency TSV-based 3D IC systems (Fang *et al.*, 2015). In addition to dielectric liner optimization, the selection of TSV core material also plays a critical role in determining electrical performance and noise behavior. Copper (Cu) is commonly used as the conventional TSV core material because of its high electrical conductivity (Hwang *et al.*, 2016). However, Cu interconnects may suffer from electromigration, increased power dissipation, and electromagnetic interference at high frequencies (Pragathi *et al.*, 2020). To overcome these limitations, alternative materials such as carbon nanotubes (CNTs) and semiconductor cores including polycrystalline silicon (Poly-Si), polycrystalline germanium (Poly-Ge), crystalline silicon (Crys-Si), crystalline germanium (Crys-Ge), and zinc oxide (ZnO) have been investigated (Kumar & Mohanraj, 2024b). Among these materials, CNT interconnects are particularly promising due to their excellent electrical conductivity, high current-carrying capability, superior thermal conductivity, and reduced electromagnetic interference, making them suitable for next-generation nanoscale interconnect applications (Cho *et al.*, 2011). Several researchers have investigated techniques to reduce noise coupling in TSV-based 3D ICs (Prakash *et al.*, 2022). This work presents a unique noise-coupling reduction strategy that employs electrical involvement models. By reducing the electrical participation of wave-carrying to victim TSVs by 22%, this new paradigm improves system performance at higher THz frequencies (Kumar & Mohanraj, 2024a). Polymer-based dielectric materials, such as benzocyclobutene, have been shown to significantly enhance electrical isolation and minimize capacitive coupling between adjacent TSVs. Concurrently, investigations into CNT-based interconnects demonstrate that CNTs offer superior electrical performance and enhanced signal integrity over conventional copper interconnects, particularly in high-frequency applications (Aslani-Amoli *et al.*, 2022). The research analyzed the performance of metal-insulator-semiconductor and metal-semiconductor using cylindrical, tapered, annular, and square TSVs. In 32 nm technology, a CMOS-based linked driver-via-load configuration models each via

using an equivalent-circuit model comprising resistance, inductance, conductance, and capacitance for metal-insulator-semiconductor- and metal-semiconductor-based TSV forms. The manufacturing company claims that the electrical model effectively accounts for micro-bump and inter-metal dielectric effects in 32 nm technology (Chandrakar *et al.*, 2020). Transmission losses are the key issue for meeting customer demand. Transmission and distribution losses may be reduced to some extent. By deploying distributed generators and compensation devices in distribution systems, transmission system losses may be reduced. A low-temperature “via-last” technique will be presented in this study (Rafi & Dhal, 2020). This method was developed for wafer-level CMOS image sensor packing. The design rules for the vias will be briefly described, followed by the technological steps: glass wafer carrier bonding onto the silicon substrate, silicon thinning, backside technology, double-side lithography, silicon deep etching, silicon sidewall insulation, via metallization, and final bumping (Henry *et al.*, 2008). Understanding how the brain functions and how neural impulses transfer requires robust, high-quality biosignal probes. Bio-signals are weak and noisy; the sensor-CMOS connection length affects bio-signal quality (Chou *et al.*, 2014). This research examines crosstalk effects in linked ternary logic interconnects. We analyze crosstalk in paired Cu and Cu-multilayer graphene (Cu-MLG) interconnects. A typical ternary inverter is utilized to drive Cu-MLG interconnects, which are surrounded with an MLG barrier (Badugu *et al.*, 2020). Poisson’s equation was used to describe the electric field, surface charge, and silicon capacitance in relation to the surface potential of a single TSV. Electrons, holes, and ionized donor/acceptor charges in the p-type silicon substrate are included in the calculations (Chang *et al.*, 2015). Graphene nanoribbons (GNRs), single graphene sheets, have many of the interesting electrical, mechanical, and thermal characteristics of CNTs (Naeemi & Meindl, 2007). Compact physical models for GNR conductance as functions of chirality, breadth, Fermi level, and edge electron scatterings are provided. Motivated by these observations, this work presents a comprehensive comparative analysis of TSV core materials and dielectric liners to evaluate their impact on noise coupling in TSV-based 3D ICs. In this study, Cu, CNTs, and semiconductor core materials are analyzed using both SiO₂ and Teflon dielectric liners in single-liner and stacked-liner configurations. The analysis is conducted at 10 GHz and 1 THz to evaluate high-frequency signal integrity. The objective of this research is to identify an optimal TSV configuration that minimizes noise coupling and enhances isolation for next-generation high-performance 3D IC systems.

2. Through-silicon via structure and proposed model

The TSV structure mainly consists of three fundamental components: core material, dielectric liner, and silicon substrate. The core material acts as the primary conducting path for signal transmission between vertically stacked dies, while the dielectric liner provides electrical insulation between the TSV core and the surrounding silicon substrate. The silicon substrate supports the TSV structure and integrates it with the overall chip architecture. Figure 2 illustrates the TSV-based 3D IC structure, showing the copper TSV, dielectric liner, and silicon substrate, which together enable vertical interconnects between different device layers. In conventional TSV structures, Cu is widely used as the core material due to its very high electrical conductivity and well-established fabrication technology. However, Cu-based TSVs may introduce higher electromagnetic interference, thermal stress, and reliability issues, particularly under high-frequency operation. These challenges motivate the exploration of alternative materials that can improve signal integrity and reduce noise coupling

in 3D ICs.

Therefore, in this work, several alternative core materials, including CNTs, Poly-Si, Poly-Ge, Crys-Si, Crys-Ge, and ZnO, were investigated and compared with conventional copper TSVs. These materials were selected due to their unique electrical, thermal, and mechanical characteristics, which can influence the performance of TSV interconnects. Table 1 presents the electrical, thermal, and mechanical properties of the proposed core materials, which are considered to evaluate their effectiveness in reducing noise coupling in TSV-based 3D IC architectures.

3. Through-silicon via structure with its dimensions according to the International Technology Roadmap for Semiconductors guidelines

The proposed 3D IC model consists of four TSVs arranged within a silicon substrate. Among these TSVs, one TSV acts as the aggressor, which carries an electrical potential of 1 V and serves as the primary source of signal excitation. The adjacent TSV acts as the victim TSV, which is affected

Table 1. Material properties of through-silicon via core materials used in a three-dimensional integrated circuit

Properties	Units	Copper	Carbon nanotubes	Crystalline germanium	Crystalline silicon	Polycrystalline silicon	Polycrystalline germanium	Zinc oxide nanowires
Relative permittivity	1	1	~2-5	16.2	11.7	~11.7	~16.2	8.5-10
Electrical conductivity	S/m	5.998×10^7	$\sim 10^6-10^7$	2.17×10^{-6}	1.56×10^{-3}	Varies	Varies	1-10
Heat capacity at constant pressure	J/(kg.K)	385	~700	322	700	~700	~322	40
Surface emissivity	1	0.5	~0.98	0.18	0.6-0.9	0.6-0.9	0.18	0.85-0.9
Density	kg/m ³	8,940	~1,300-1,400	5,323	2,330	~2,330	~5,323	5,600
Thermal conductivity	W/(m.K)	400	~2,000-3,000	60.2	148	~100	~60.2	0.6-1.0
Young's modulus	Pa	126×10^9	$\sim 1 \times 10^{12}$	102×10^9	130×10^9	$\sim 130 \times 10^9$	$\sim 102 \times 10^9$	140×10^9
Poisson's ratio	1	0.34	~0.19	0.28	0.28	~0.28	~0.28	0.35
Reference resistivity	ohm.m	1.667×10^{-8}	$\sim 10^{-6}-10^{-5}$	4.6×10^{-1}	6.4×10^2	$\sim 10^{-3}-10^2$	$\sim 4.6 \times 10^{-1}$	10^4-10^6

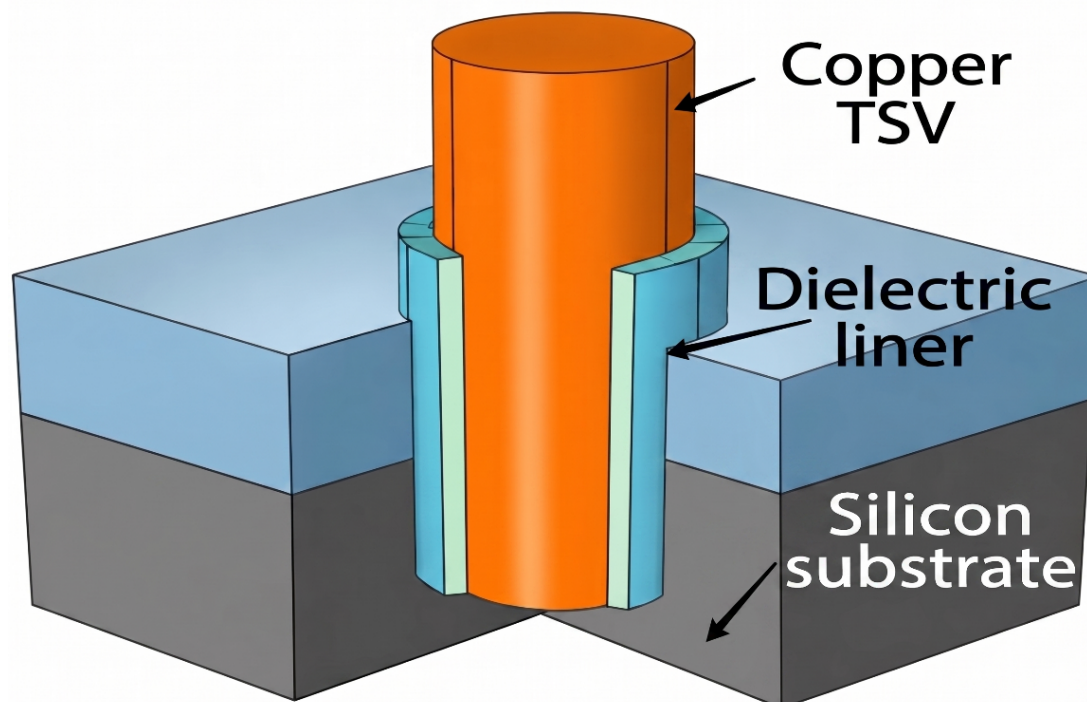


Figure 2. Three-dimensional schematic of the through-silicon via (TSV)-based three-dimensional integrated circuit structure showing copper TSV, dielectric liner, and silicon substrate used for electro-thermal analysis. Created by the authors using COMSOL Multiphysics® v6.x.

by noise coupling induced by the aggressor TSV through the surrounding dielectric and silicon substrate. The remaining two TSVs are configured as ground TSVs to provide a reference potential and to reduce electromagnetic interference within the structure. This configuration enables the analysis of noise coupling behavior between aggressor and victim TSVs in a 3D IC environment. The entire TSV-based 3D IC structure is designed according to the International Technology Roadmap for Semiconductors guidelines, ensuring realistic geometrical dimensions and material parameters suitable for high-frequency interconnect analysis.

Table 2 details the specific physical dimensions, such as a 2 μm diameter and 8 μm height, required to model the electrical behavior and signal integrity of the TSV structure. These geometric constraints, including the dielectric liner thickness and pitch, serve as the foundational boundary conditions for the simulation environment (Table 2).

Figure 3 illustrates the final 3D IC structure designed according to the guidelines of the International Technology Roadmap for Semiconductors. The model represents a single block of a 3D IC implemented for analyzing electrical behavior and noise coupling in TSV-based architectures. The structure consists of a silicon substrate block in

which four cylindrical TSVs are vertically embedded. Each TSV has a diameter of 2 μm and a height of 8 μm , while the center-to-center spacing between TSVs is 4 μm . Around each TSV, a dielectric liner of thickness 0.15 μm is provided to electrically isolate the conductive TSV from the surrounding silicon substrate.

Among the four TSVs, one TSV was configured as the aggressor TSV, which carries the signal excitation (1 V input). The adjacent TSV acts as the victim TSV, which experiences noise due to capacitive and conductive coupling through the silicon substrate and dielectric liner. The remaining two TSVs were configured as ground TSVs, which help in providing a reference potential and reducing electromagnetic interference within the structure.

The upper portion of the structure represents the active device layer (IC block), where circuit elements are placed. In this work, the core material of the active region was varied to study its impact on noise coupling, electric field distribution, and signal integrity in the TSV-based 3D IC structure. By changing the core material properties, such as dielectric constant and conductivity, the coupling behavior between aggressor and victim TSVs can be analyzed and optimized. The color contour shown in the model represents the normalized electric potential distribution,

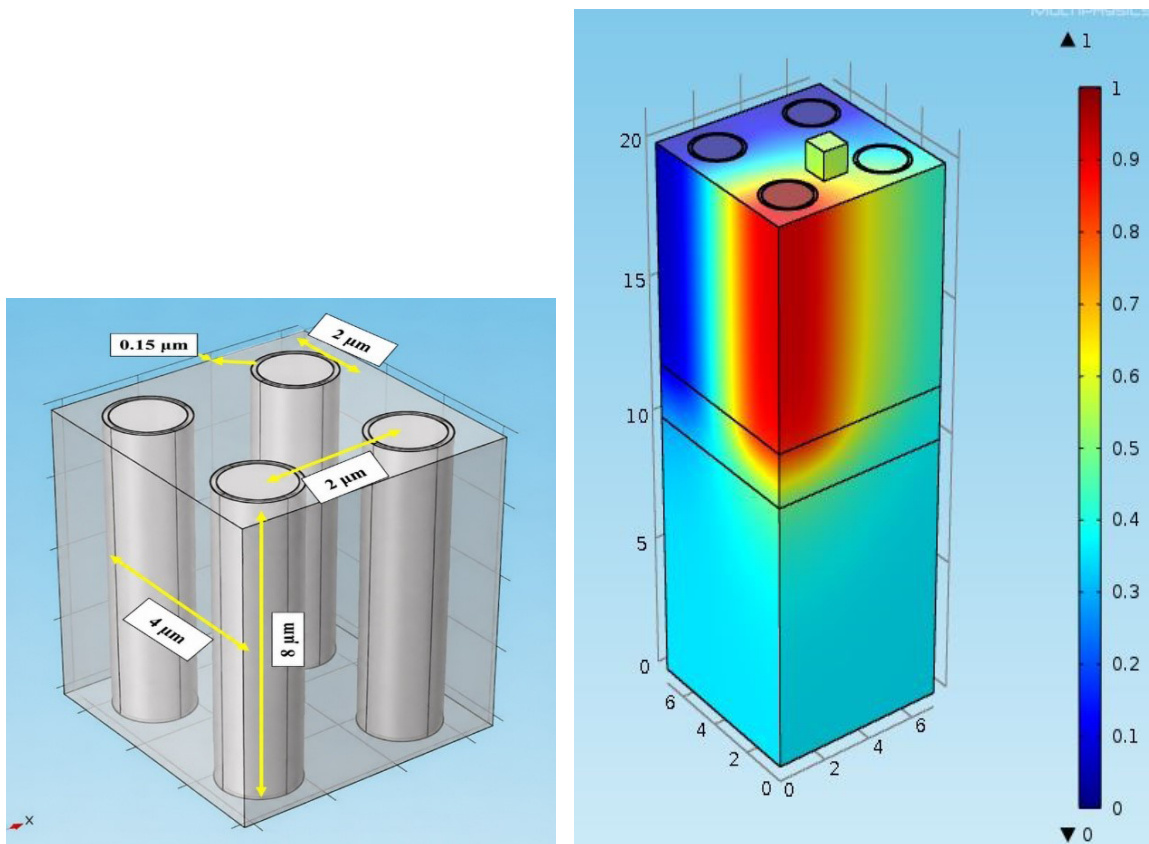


Figure 3. Three-dimensional view of potential variation using stacked layers of liner for multiple integrated circuits

ranging from 0 to 1, where red indicates the maximum potential near the aggressor TSV and blue represents the minimum potential regions. The gradual transition of colors across the structure indicates the propagation of the electric field and coupling effects within the silicon substrate and surrounding dielectric materials.

Table 2. Through-silicon via (TSV) geometric parameters used in the simulation

Parameter	Distance
TSV diameter	2 μm
TSV height	8 μm
Dielectric liner thickness	0.15 μm
TSV pitch	2 μm
Silicon substrate thickness	2 μm
Distance between TSVs	4 μm

This model was used to evaluate how different core materials influence noise propagation and coupling effects in high-frequency 3D IC designs, enabling the identification of materials that improve signal integrity and reduce interference in advanced ICs.

4. Results and discussion

In this work, the electrical behavior of the proposed TSV-based 3D IC model was analyzed using different dielectric liner configurations and operating frequencies. The study considered two dielectric liner structures: a single liner and a stacked liner. Two operating frequencies, 10 GHz and 1 THz, were used to investigate the effect of frequency scaling on noise coupling and signal propagation. Two dielectric materials were used as liner materials: SiO₂ and Teflon. In addition, six different core materials (Cu, Poly-Si, Poly-Ge, Crys-Si, Crys-Ge, ZnO, and CNTs) were used in the active region of the IC block to evaluate their influence on electrical coupling and field distribution. The simulation results were analyzed in terms of electric potential distribution, coupling behavior, and signal propagation characteristics between aggressor and victim TSVs.

4.1. Single liner with silicon dioxide at 10 GHz

Figure 4 shows the electric potential variation for the TSV structure using a single liner of SiO₂ at 10 GHz with different core materials. The potential started at 1 V at the aggressor TSV (0 μm) and gradually decreased toward the victim TSV. At the victim TSV (4 μm), the lowest potential was observed for CNT with a value of approximately 0.37 V, while the highest potential occurred for Cu at about 0.67 V. The corresponding attenuation values were approximately -8.6 dB for CNT and -4.3 dB for Cu. The higher attenuation in CNT indicates lower coupling noise between TSVs.

4.2. Single liner with silicon dioxide at 1 THz

Figure 5 shows the electric potential variation along the arc length for a single liner of SiO₂ at 1 THz with different core materials. The potential began at 1 V at the aggressor TSV and decreased gradually toward the victim TSV. At the victim TSV (4 μm), the lowest potential was observed for CNT with approximately 0.41 V, while the highest potential occurred for Cu at about 0.67 V. The corresponding attenuation values were approximately -7.7 dB for CNT and -3.5 dB for Cu. The larger attenuation for CNT indicates reduced coupling between aggressor and victim TSVs.

4.3. Single liner with Teflon at 10 GHz

Figure 6 shows the electric potential variation for the TSV structure using a single liner of Teflon at 10 GHz with different core materials. The potential started at 1 V at the aggressor TSV (0 μm) and gradually decreased toward the victim TSV. At the victim TSV (4 μm), the lowest potential was observed for CNT with a value of approximately 0.37 V, while the highest potential occurred for Cu at about 0.67 V. The corresponding attenuation values were approximately -8.63 dB for CNT and -8.18 dB for Cu. The higher attenuation in CNT indicates lower coupling noise between TSVs.

4.4. Single liner with Teflon at 1 THz

Figure 7 shows the electric potential variation for the TSV structure using a single liner of Teflon at 10 GHz with different core materials. The potential started at 1 V at the aggressor TSV (0 μm) and gradually decreased toward the victim TSV. At the victim TSV (4 μm), the lowest potential was observed for CNT with a value of approximately 0.28 V, while the highest potential occurred for Poly-Ge at approximately 0.58 V. The corresponding attenuation values were approximately -11.06 dB for CNT and -4.73 dB for Poly-Ge. The higher attenuation in CNT indicates lower coupling noise between TSVs.

4.5. Stacked liner with silicon dioxide at 10 GHz

Figure 8 shows the electric potential variation for the TSV structure using a stacked liner of SiO₂ at 10 GHz with different core materials. The potential started at 1 V at the aggressor TSV (0 μm) and gradually decreased toward the victim TSV. At the victim TSV (4 μm), the lowest potential was observed for CNT with a value of approximately 0.33 V, while the highest potential occurred for Cu at about 0.59 V. The corresponding attenuation values were approximately -9.63 dB for CNT and -4.58 dB for Cu. The higher attenuation in CNT indicates lower coupling noise between TSVs.

4.6. Stacked liner with silicon dioxide at 1 THz

Figure 9 shows the electric potential variation for the TSV structure using a stacked liner of SiO₂ at 1 THz with different core materials. The potential started at 1 V at the aggressor TSV (0 μm) and gradually decreased toward the victim TSV. At the victim TSV (4 μm), the lowest potential was observed for CNT with a value of approximately 0.31 V, while the highest potential occurred for Cu at about 0.57 V. The corresponding attenuation values were approximately -10.17 Db for CNT and -4.88 dB for Cu. The higher attenuation in CNT indicates lower coupling noise between TSVs.

4.6. Stacked liner with Teflon at 10 GHz

Figure 10 shows the electric potential variation for the TSV structure using a stacked liner of Teflon at 10 GHz with different core materials. The potential started at 1 V at the aggressor TSV (0 μm) and gradually decreased toward the victim TSV. At the victim TSV (4 μm), the lowest potential was observed for CNT with a value of approximately 0.31 V, while the highest potential occurred for Cu at about 0.66 V. The corresponding attenuation values were approximately -10.46 dB for CNT and -3.61 dB for Cu. The higher attenuation in CNT indicates lower coupling noise between TSVs.

4.6. Stacked liner with Teflon at 1 THz

Figure 11 shows the electric potential variation for the TSV structure using a stacked liner of Teflon at 1 THz with different core materials. The potential started at 1 V at the aggressor TSV (0 μm) and gradually decreased toward the victim TSV. At the victim TSV (4 μm), the lowest potential was observed for CNT, with a value of approximately 0.22 V, while the highest potential occurred for Cu at about 0.63 V. The corresponding attenuation values were approximately -13.56 dB for CNT and -8.53 dB for Cu. The higher attenuation in CNT indicates lower coupling noise between TSVs.

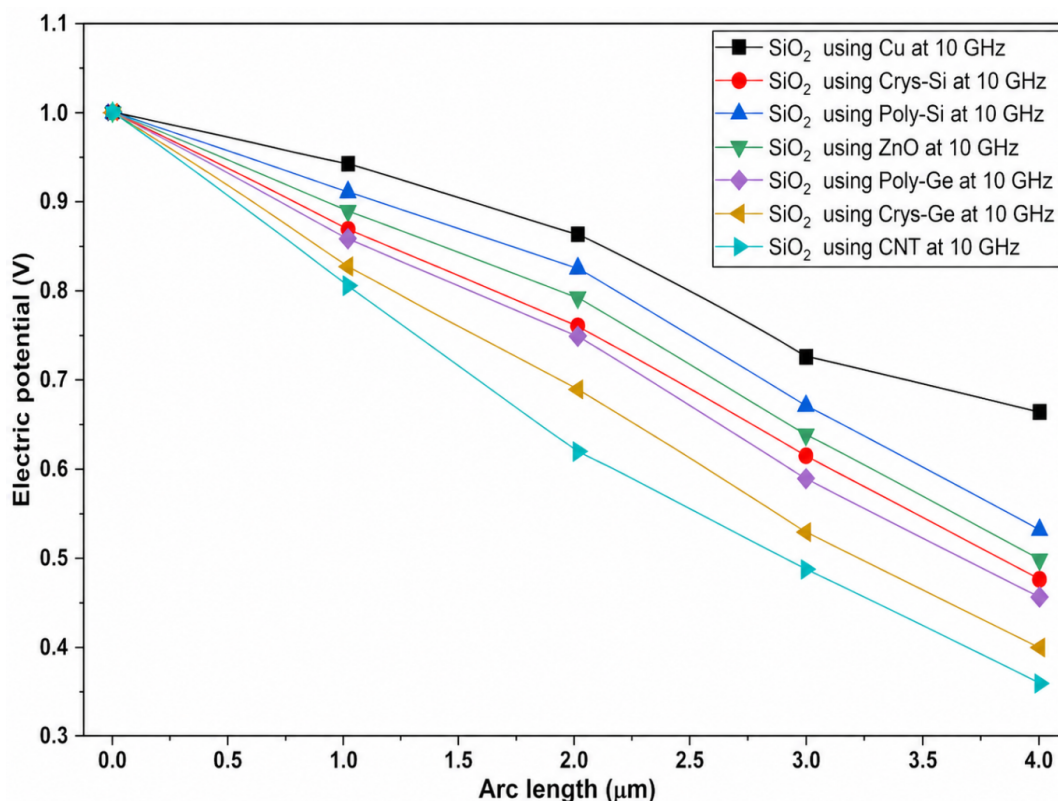


Figure 4. Electric potential variation along arc length for a single silicon dioxide liner at 10 GHz with different core materials, including copper (Cu) and carbon nanotube (CNT)

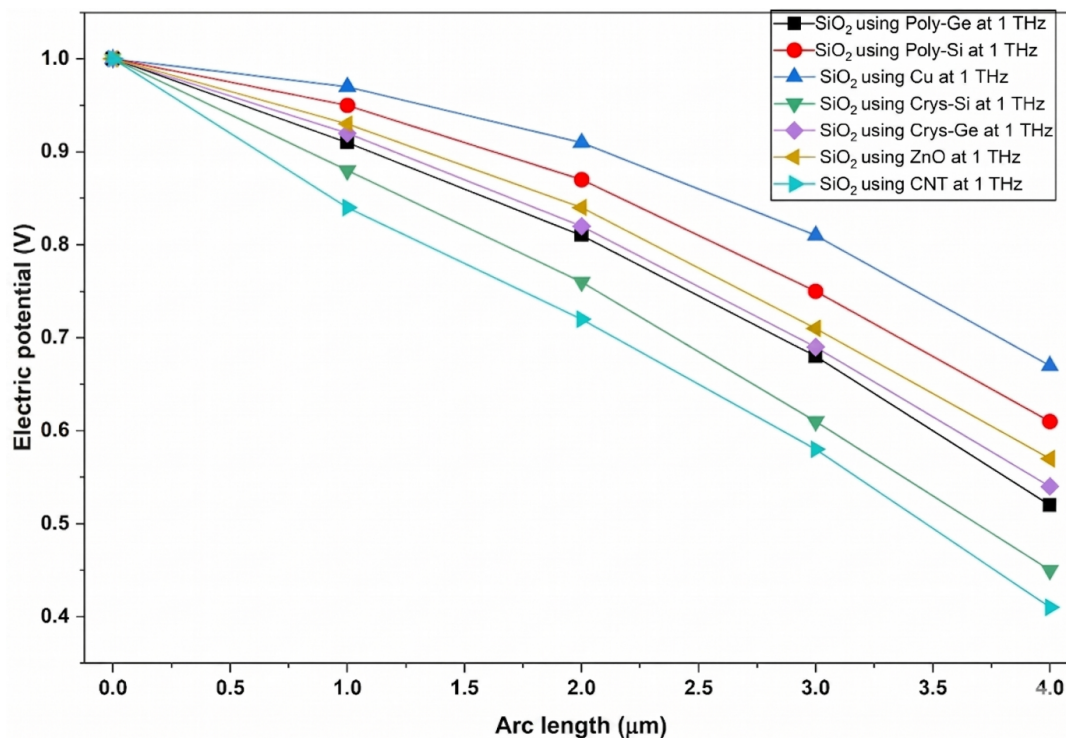


Figure 5. Electric potential variation along arc length for a single silicon dioxide liner at 1 THz using different core materials

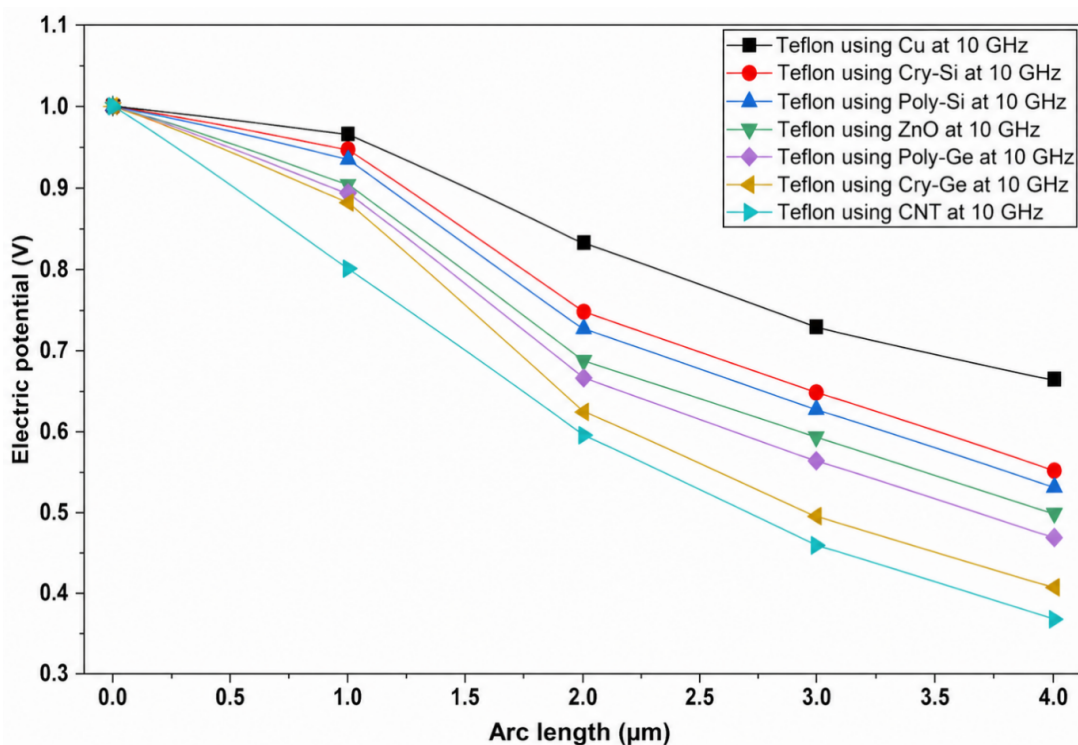


Figure 6. Electric potential variation along arc length for a single liner with Teflon at 10 GHz with different core materials, including copper (Cu) and carbon nanotube (CNT)

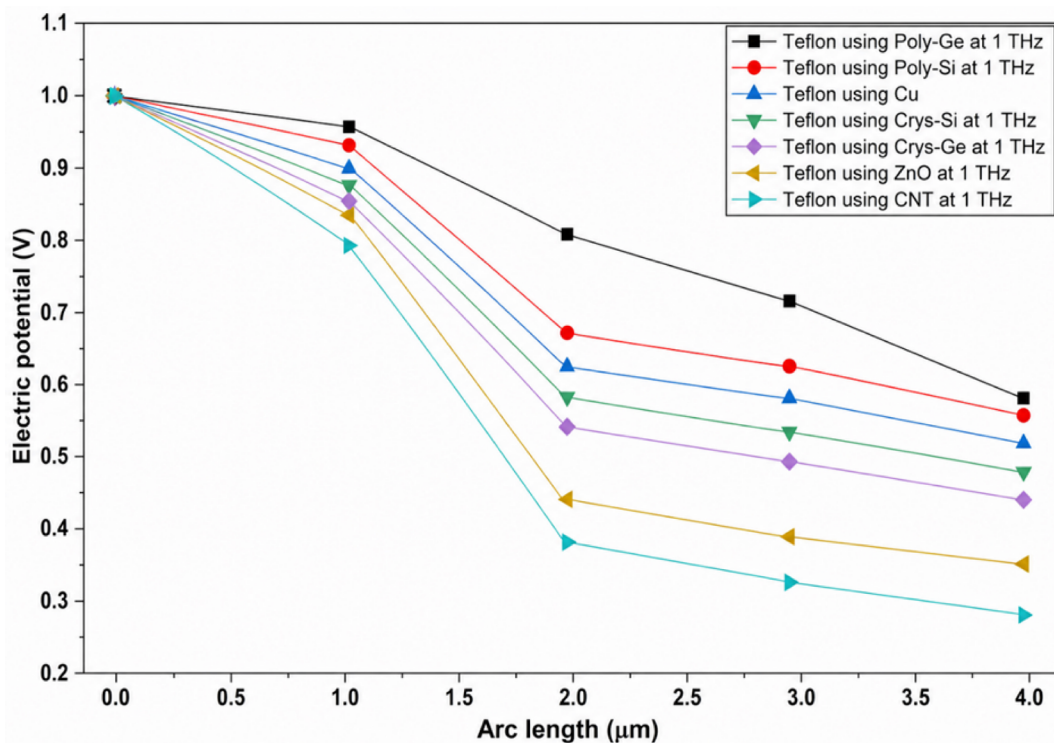


Figure 7. Electric potential variation along arc length for a single liner with Teflon at 1 THz with different core materials, including Poly-Ge and carbon nanotube (CNT)

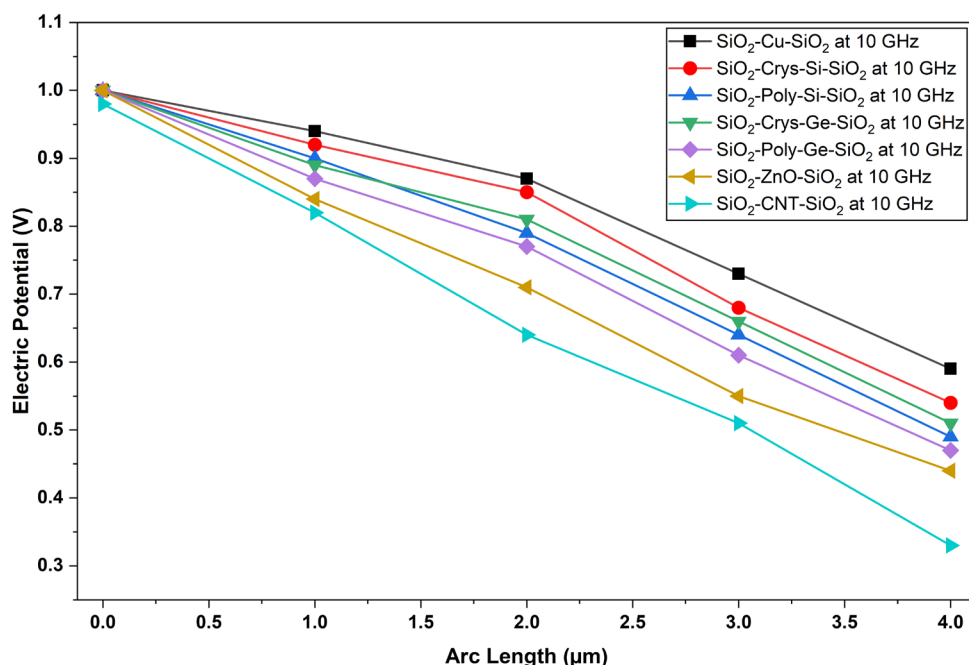


Figure 8. Electric potential variation along arc length for a stacked liner with silicon dioxide at 10 GHz with different core materials, including copper (Cu) and carbon nanotube (CNT)

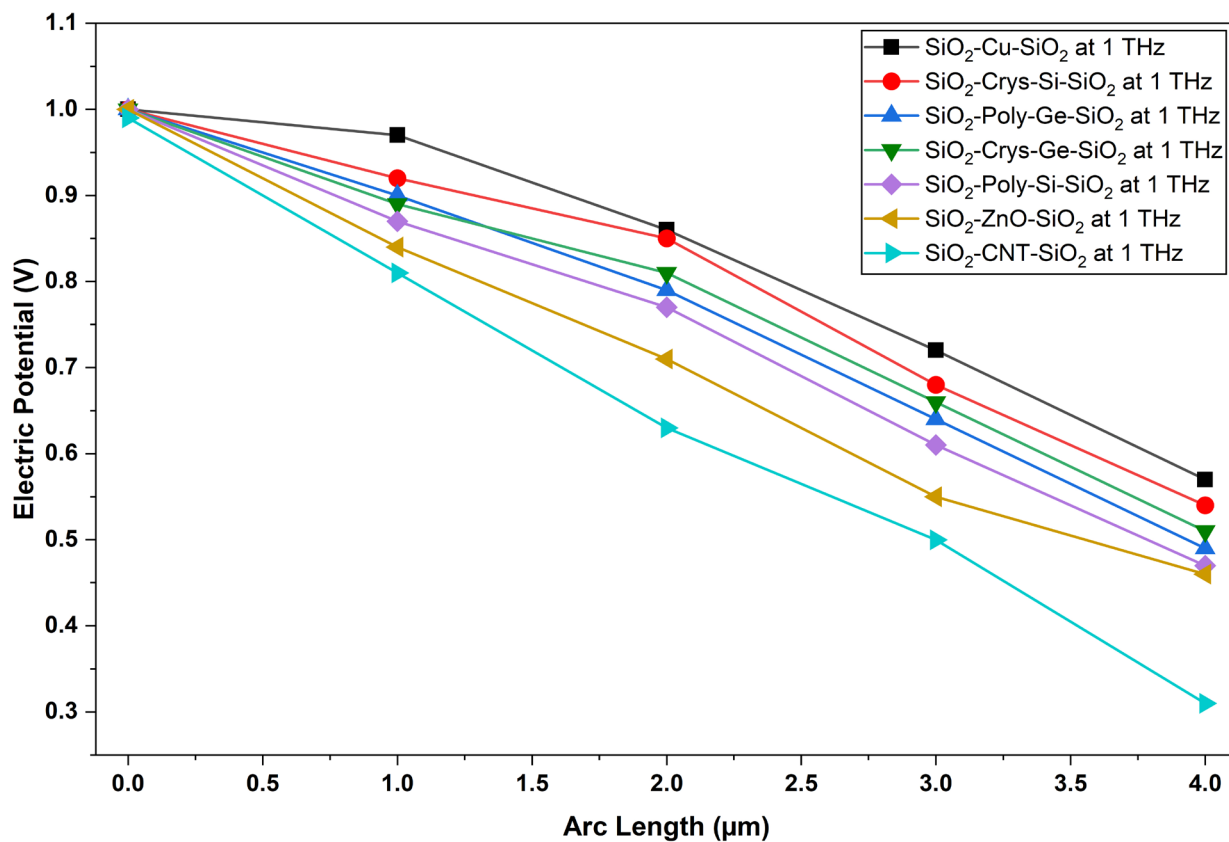


Figure 9. Electric potential variation along arc length for a stacked liner with silicon dioxide (SiO₂) at 1 THz with different core materials, including copper (Cu) and carbon nanotube (CNT)

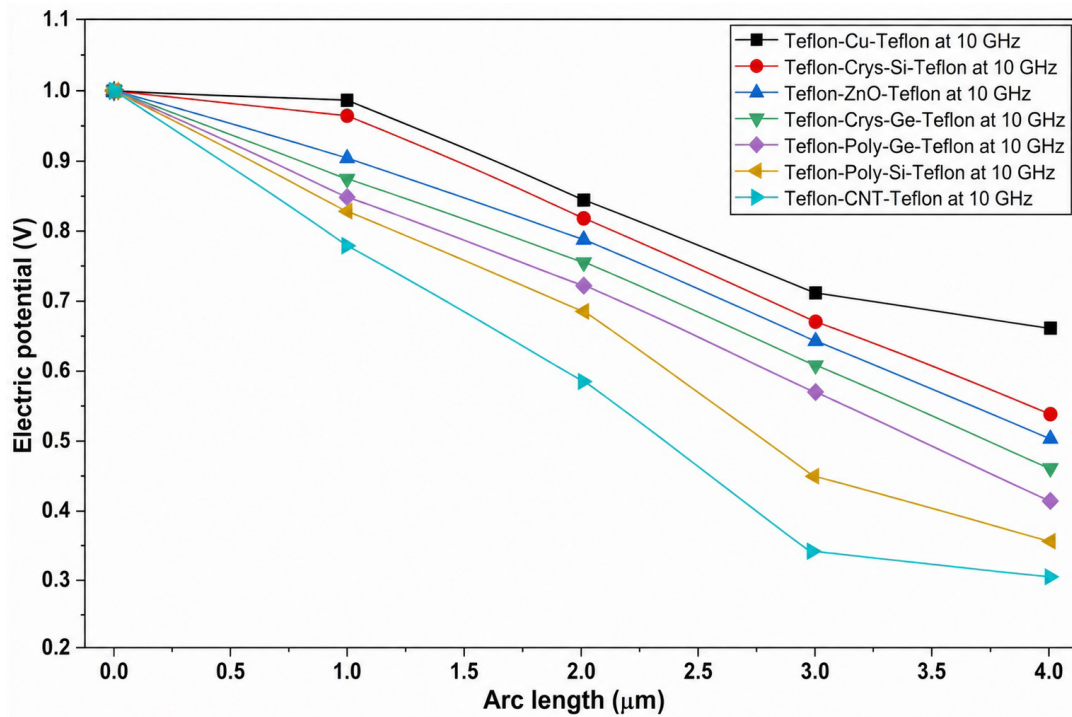


Figure 10. Electric potential variation along arc length for a stacked liner with Teflon at 10 GHz with different core materials, including copper (Cu) and carbon nanotube (CNT)

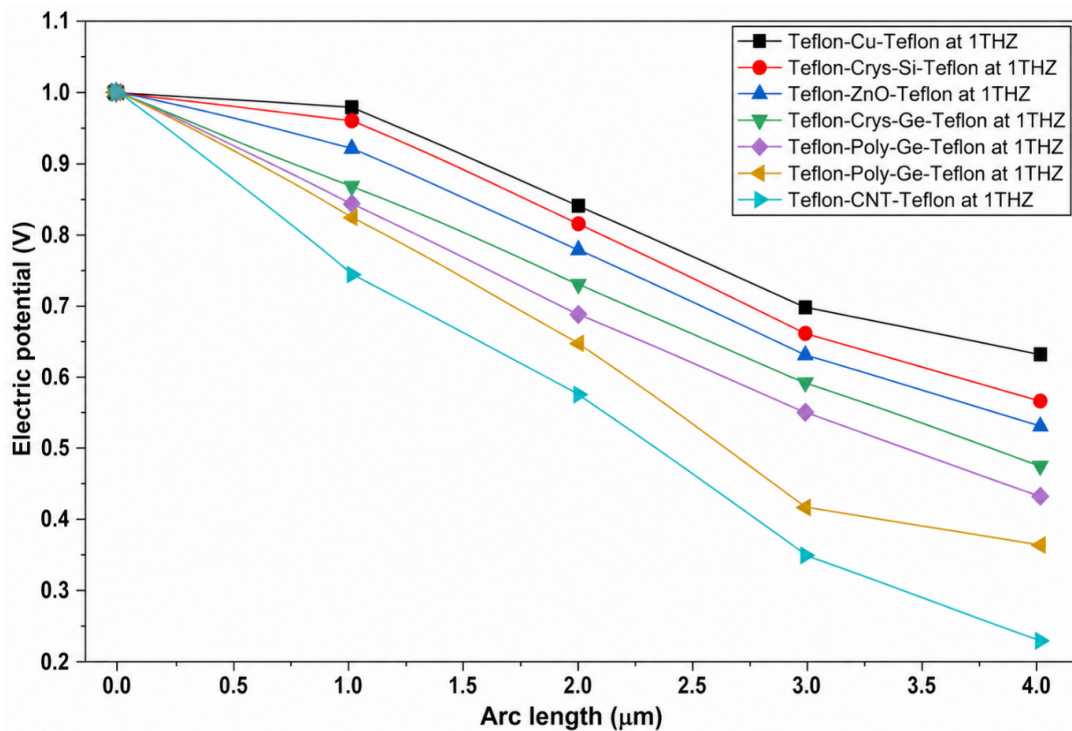


Figure 11. Electric potential variation along arc length for a stacked liner with Teflon at 1 THz with different core materials, including copper (Cu) and carbon nanotube (CNT)

5. Conclusion

This study analyzed noise coupling in TSV-based 3D IC structures using different liner and interlayer materials at high frequencies. The results show that the stacked liner configuration significantly improves signal isolation compared to conventional structures. Among the investigated materials, the combination of polytetrafluoroethylene (Teflon) liner with a CNT interlayer demonstrates the best performance. At a distance of 4 μm (victim TSV), this configuration achieved the highest attenuation of approximately -13.56 dB, indicating superior suppression of noise coupling. The CNT interlayer consistently outperforms Cu due to its favorable electromagnetic characteristics at 1 THz. Although SiO_2 is widely used in semiconductor technology, the Teflon-based stacked liner provided higher attenuation (-13.56 dB compared to -8.53 dB) for SiO_2 with CNT. Therefore, the Teflon-CNT stacked liner structure was identified as the most effective configuration for reducing noise coupling and improving signal integrity in high-frequency TSV-based 3D IC systems.

Acknowledgments

None.

Funding

None.

Conflict of interest

The authors declare they have no competing interests.

Author contributions

Conceptualization: Prathap Reddy Pathakunta Guru, Sravan Abhilash Kothapalli

Formal analysis: Prathap Reddy Pathakunta Guru, Sravan Abhilash Kothapalli

Investigation: Prathap Reddy Pathakunta Guru, Sravan Abhilash Kothapalli

Methodology: Prathap Reddy Pathakunta Guru

Visualization: Prathap Reddy Pathakunta Guru

Writing—original draft: Prathap Reddy Pathakunta Guru

Writing—review & editing: Prathap Reddy Pathakunta Guru, Sravan Abhilash Kothapalli

Availability of data

All data generated or analyzed during this study are included in this published article.

References

Aslani-Amoli, N., ur Rehman, M., Liu, F., Swaminathan, M.,

Zhuang, C.-G., Zhelev, N. Z., Seok, S.-H., & Kim, C. (2022). Characterization of alumina ribbon ceramic substrates for 5G and mm-wave applications. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 12(9), 1432–1445.

<https://doi.org/10.1109/tcpmt.2022.3196663>

Avouris, P., Chen, Z., & Perebeinos, V. (2007). Carbon-based electronics. *Nature Nanotechnology*, 2(10), 605–615.

<https://doi.org/10.1038/nnano.2007.300>

Badugu, D. M., & S, S. (2020). Crosstalk reduction in copper on-chip interconnects with graphene barrier for ternary logic applications. *International Journal of Circuit Theory and Applications*, 48(12), 2097–2110.

<https://doi.org/10.1002/cta.2809>

Cadence PCB Solutions. (2018). *3D ICs with TSVs – Design Challenges and Requirements*. Cadence Design Systems. Accessed March 20, 2026. Available at: <https://resources.pcb.cadence.com/sigrity-whitepapers/3dics-with-tsvs-design-challenges-and-requirements>

Cao, W., Chu, J. H., Parto, K., & Banerjee, K. (2021). A mode-balanced reconfigurable logic gate built in a van der Waals strata. *npj 2D Materials and Applications*, 5(1), 20.

<https://doi.org/10.1038/s41699-020-00198-6>

Chandrakar, M., & Majumder, M. K. (2022). Impact of polymer liners on crosstalk induced delay of different TSV shapes. *IETE Journal of Research*, 70(1), 686–699.

<https://doi.org/10.1080/03772063.2022.2108915>

Chandrakar, S., Gupta, D., & Majumder, M. K. (2020). Role of through silicon via in 3D integration: Impact on delay and power. *Journal of Circuits, Systems and Computers*, 30(3), 2150051.

<https://doi.org/10.1142/S0218126621500511>

Chang, Y. Y., Ko, C. T., Yu, T. H., Hsieh, Y. S., & Chen, K. N. (2015). Modeling and characterization of TSV capacitor and stable low-capacitance implementation for wide-I/O application. *IEEE Transactions on Device and Materials Reliability*, 15(2), 129–135.

<https://doi.org/10.1109/TDMR.2015.2397698>

Cho, J., Song, E., Yoon, K., Pak, J. S., Kim, J., Lee, W., Song, T., Kim, K., Lee, J., Lee, H., Park, K., Yang, S., Suh, M., Byun, K., & Kim, J. (2011). Modeling and analysis of through-silicon via (TSV) noise coupling and suppression using a guard ring. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 1(2), 220–233.

<https://doi.org/10.1109/tcpmt.2010.2101892>

Chou, L.-C., Lee, S.-W., Huang, P.-T., Chang, C.-W., Chiang, C.-H., Wu, S.-L., Chuang, C.-T., Chiou, J.-C., Hwang, W., Wu, C.-H., Chen, K.-H., Chiu, C.-T., Tong, H.-M., & Chen, K.-N. (2014). A TSV-based bio-signal package with μ -probe

- array. *IEEE Electron Device Letters*, 35(2), 256–258.
<https://doi.org/10.1109/led.2013.2293399>
- Fang, R., Sun, X., Miao, M., & Jin, Y. (2015). Characteristics of coupling capacitance between signal-ground TSVs considering MOS effect in silicon interposers. *IEEE Transactions on Electron Devices*, 62(12), 4161–4168.
<https://doi.org/10.1109/TED.2015.2494538>
- Henry, D., Jacquet, F., Neyret, M., Baillin, X., Enot, T., Lapras, V., Brunet-Manquat, C., Charbonnier, J., Aventurier, B., & Sillon, N. (2008). Through silicon vias technology for CMOS image sensors packaging. In *2008 58th Electronic Components and Technology Conference* (pp. 556–562). IEEE.
<https://doi.org/10.1109/ectc.2008.4550028>
- Hu, J., Li, D., Liu, M., & Zhu, Z. (2019). A 10-kS/s 625-Hz-bandwidth 65-dB SNDR second-order noise-shaping SAR ADC for biomedical sensor applications. *IEEE Sensors Journal*, 20(23), 13881–13891.
<https://doi.org/10.1109/JSEN.2019.2949641>
- Hwang, C., Achkir, B., & Fan, J. (2016). Capacitance-enhanced through-silicon via for power distribution networks in 3D ICs. *IEEE Electron Device Letters*, 37(4), 478–481.
<https://doi.org/10.1109/LED.2016.2535123>
- Koester, S. J., Young, A. M., Yu, R. R., Purushothaman, S., Chen, K.-N., La Tulipe, D. C., Rana, N., Shi, L., Wordeman, M. R., & Sprogis, E. J. (2008). Wafer-level 3D integration technology. *IBM Journal of Research and Development*, 52(6), 583–597.
<https://doi.org/10.1147/jrd.2008.5388565>
- Kumar, M. S., & Mohanraj, J. (2024a). Electrical signal interference minimization using appropriate core material for 3D integrate circuit at high frequency applications. *International Journal of Electrical & Computer Engineering*, 14(3), 2500–2507.
<https://doi.org/10.11591/ijece.v14i3.pp2500-2507>
- Kumar, M. S., & Mohanraj, J. (2024b). Enhancement of liner materials based on nanomaterials to promote sustainability in noise intercourse. *International Journal of Informatics and Communication Technology*, 13(3), 476–483.
<https://doi.org/10.11591/ijict.v13i3.pp476-483>
- Naeemi, A., & Meindl, J. D. (2007). Conductance modeling for graphene nanoribbon (GNR) interconnects. *IEEE Electron Device Letters*, 28(5), 428–431.
<https://doi.org/10.1109/LED.2007.895452>
- Pragathi, D., Rakesh, B., Kumar, P. S., Vignesh, N. A., Padma, T., & Panigrahy, A. K. (2020). Noise performance improvement in 3D IC integration utilizing different dielectric materials. *Materials Today: Proceedings*, 33, 3117–3123.
<https://doi.org/10.1016/j.matpr.2020.03.737>
- Prakash, M. D., Krsihna, B. V., Satyanarayana, B. V. V., Vignesh, N. A., Panigrahy, A. K., & Ahmadsaidulu, S. (2022). A study of an ultrasensitive label free silicon nanowire FET biosensor for cardiac troponin I detection. *Silicon*, 14(10), 5683–5690.
<https://doi.org/10.1007/s12633-021-01352-5>
- Rafi, V., & Dhal, P. K. (2020). Loss minimization based distributed generator placement at radial distributed system using hybrid optimization technique. In: *2020 International Conference on Computer Communication and Informatics (ICCCI)* (pp. 1–6). IEEE.
<https://doi.org/10.1109/iccci48352.2020.9104145>
- Rafi, V., Dhal, P. K., Rajesh, M., Srinivasan, D. R., Chandrashekhar, M., & Reddy, N. M. (2023). Optimal placement of time-varying distributed generators by using crow search and black widow-hybrid optimization. *Measurement: Sensors*, 30, 100900.
<https://doi.org/10.1016/j.measen.2023.100900>
- Wang, Y., Kim, J. C., Wu, R. J., Martinez, J., Song, X., Yang, J., Zhao, Mkhoyan, Jeong & Chhowalla, M. (2019). Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature*, 568(7750), 70–74.
<https://doi.org/10.1038/s41586-019-1052-3>
- Xu, Y., Zeng, Y., Zhao, Y., Lee, C., He, M., & Liu, Z. (2025). A review of mechanism and technology of hybrid bonding. *Journal of Electronic Packaging*, 147(1), 010801.
<https://doi.org/10.1115/1.4065650>
- Yasmin, S., Kumar, G. V. N., Rafi, V., Yamuna, P., & Sailaja, K. (2022). Design of bi-directional charger for electric vehicle. In *2022 International Conference on Advances in Computing, Communication and Materials (ICACCM)* (pp. 1–6). IEEE.
<https://doi.org/10.1109/icaccm56405.2022.10009204>
- Zheng, J.-C., Zhang, L., Kretinin, A. V., Morozov, S. V., Wang, Y. B., Wang, T., Li, X., Ren, F., Zhang, J., Lu, C.-Y., Chen, J.-C., Lu, M., Wang, H.-Q., Geim, A. K., & Novoselov, K. S. (2016). High thermal conductivity of hexagonal boron nitride laminates. *2D Materials*, 3(1), 011004.
<https://doi.org/10.1088/2053-1583/3/1/011004>